Power-Aware System-on-Chip Test Planning

Erik Larsson

Department of Computer Science

Linköping University

Sweden

LiU expanding reality

Test and Power Consumption

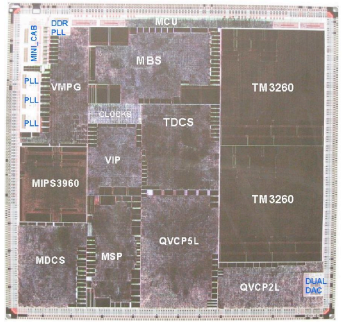
- IC manufacturing not perfect
- Testing separates good ICs from bad ICs
- To reduce cost, test time should be minimized
- Circuit activity (related to power consumption) goes high
- Circuit activity higher in test mode than that in functional mode
- But ICs are designed for functional mode power consumption
- Correct operation of the IC cannot be guaranteed at high power consumption
- A good IC can be classified as faulty; leading to low yield and higher cost
- Need to address test power consumption

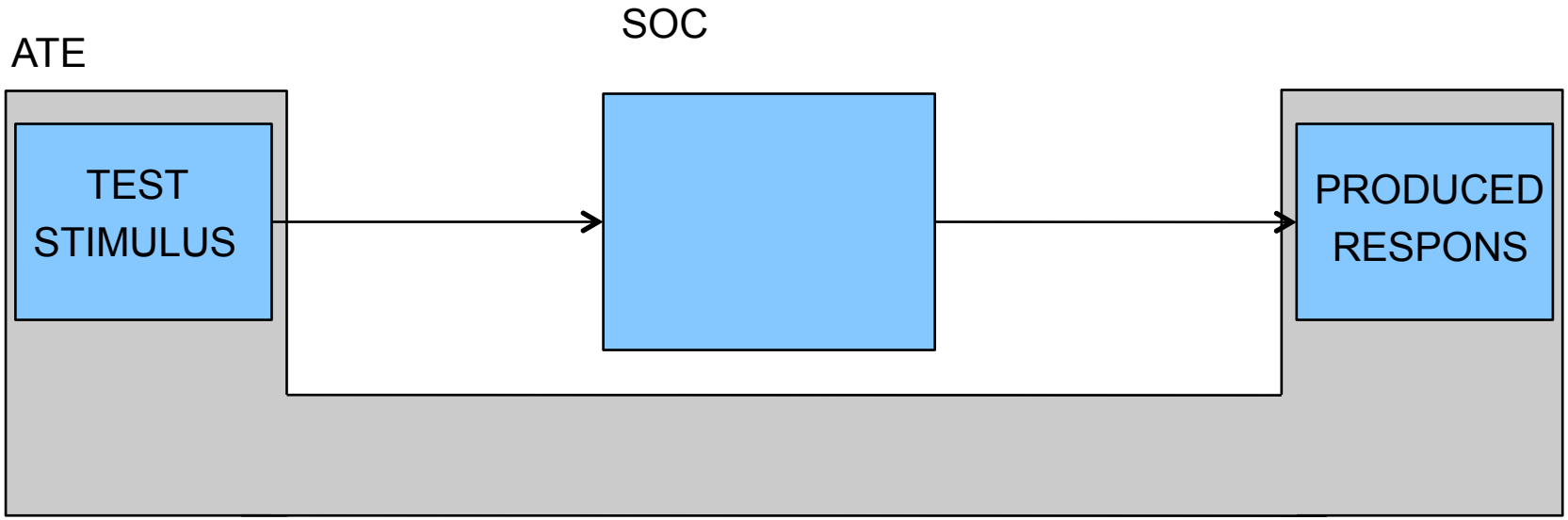
C. Shi and R. Kapur, "How Power Aware Test Improves Reliability and Yield," IEEDesign.com, September 15, 2004.

Outline

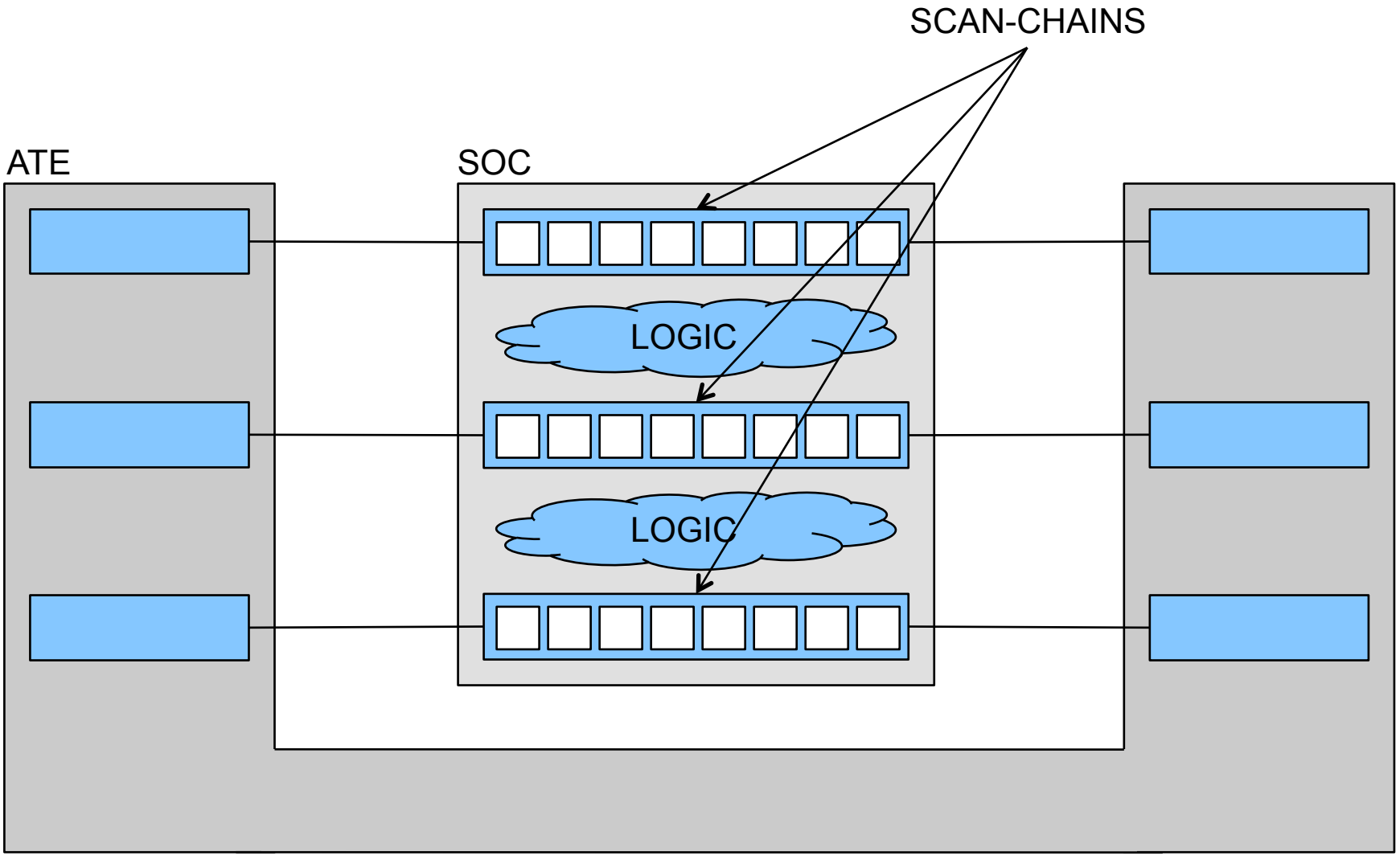
- Introduction
- Test Planning core-based SOCs
- Test Planning + Power-Aware DfT
- Conclusions and Perspectives

IC Test

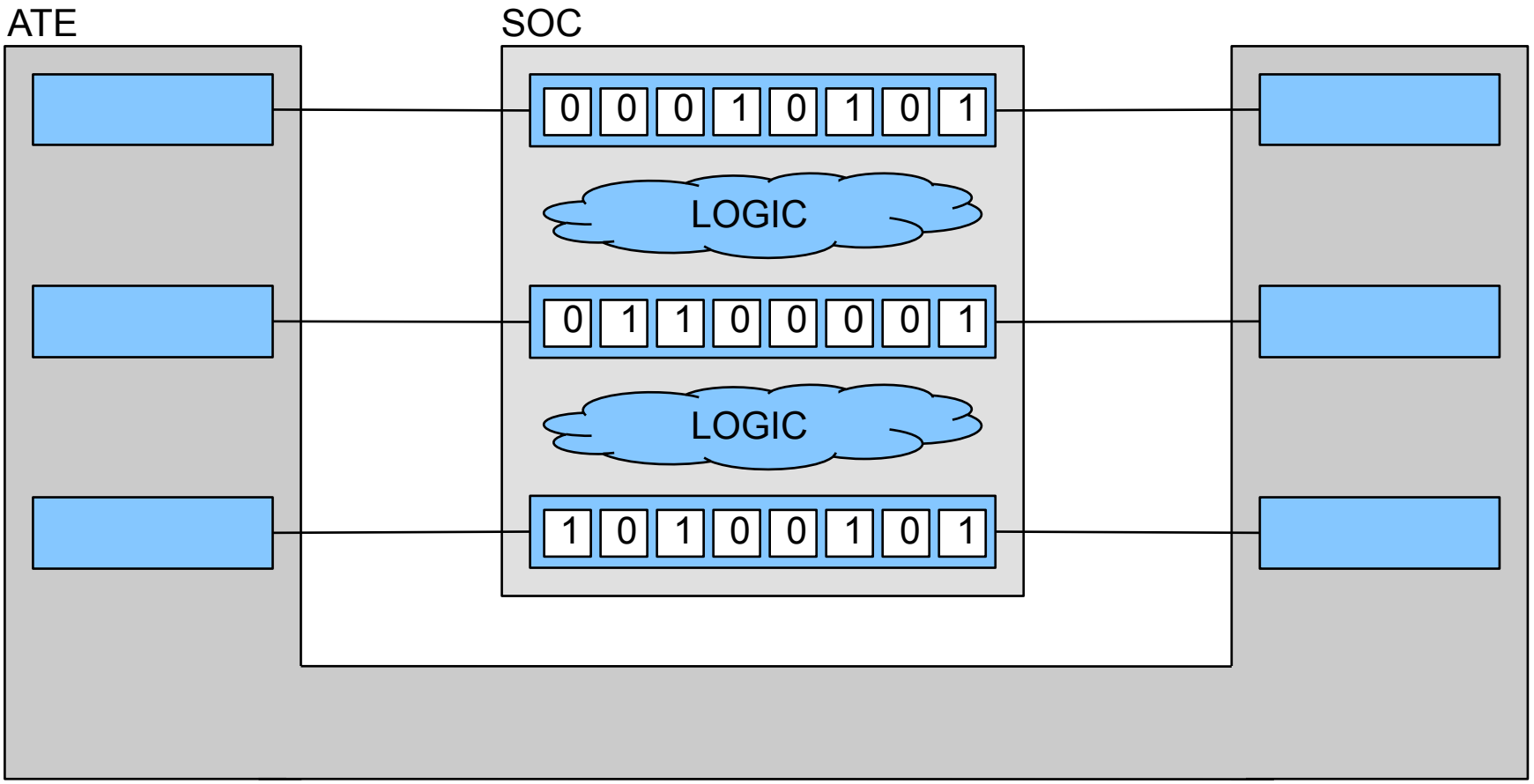

MCU
MBS
VMPG
TM3260
TDCS
VIP
MIPS3960
TM3260
QVCP5L
MDCS
MSP
QVCP2L


ATE
SOC
TEST STIMULUS
PRODUCED RESPONS

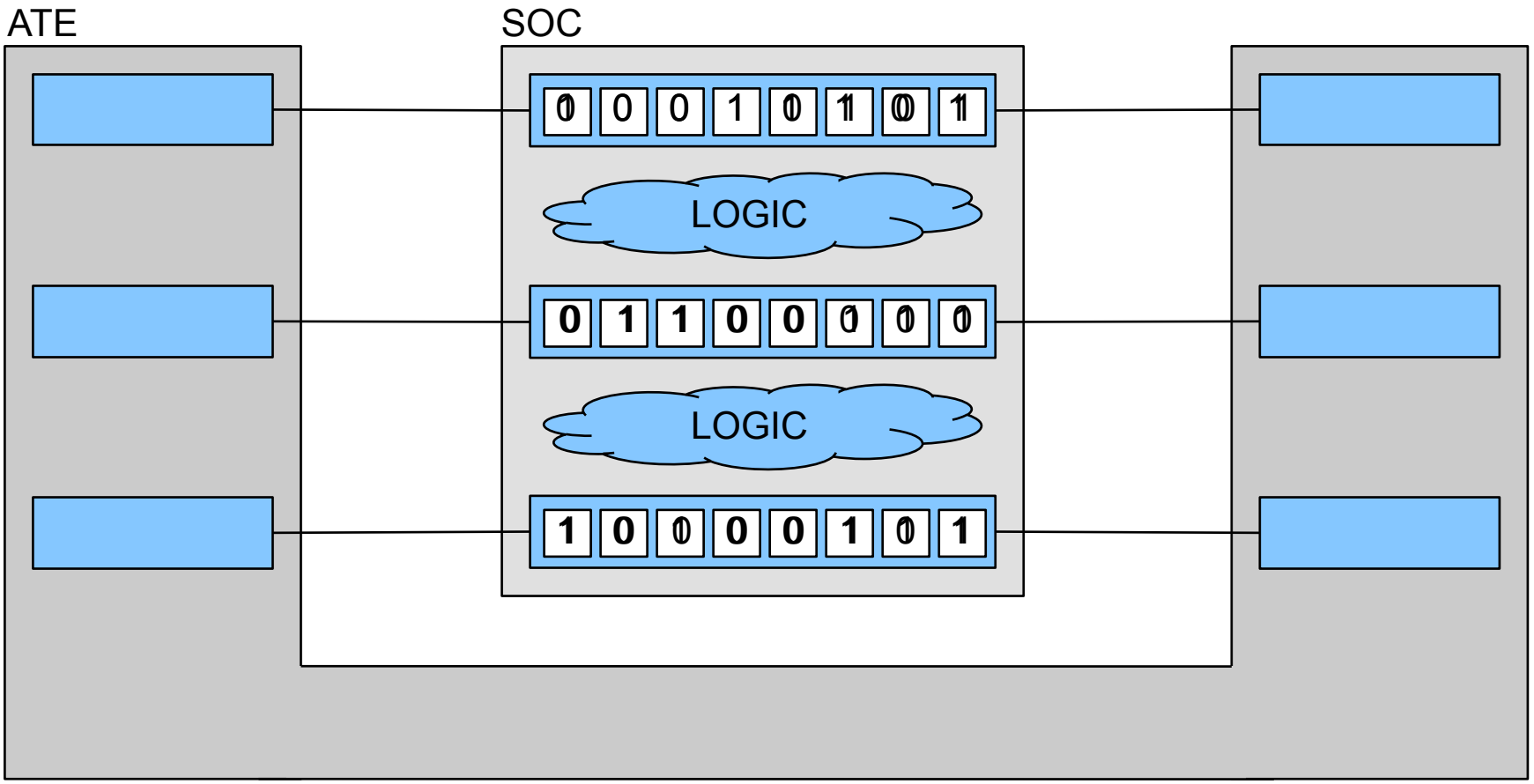
IC Test



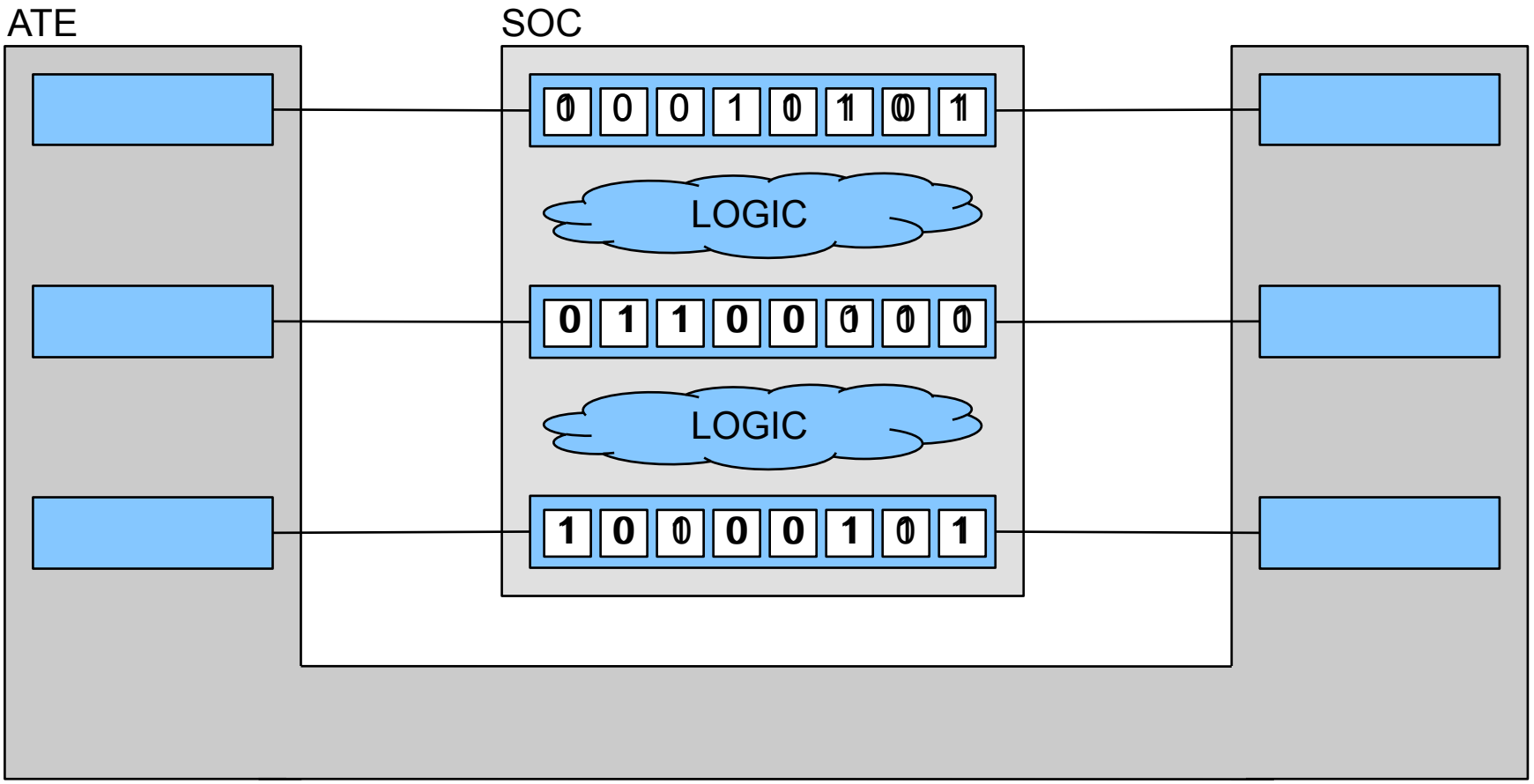
Shift-In Stimulus



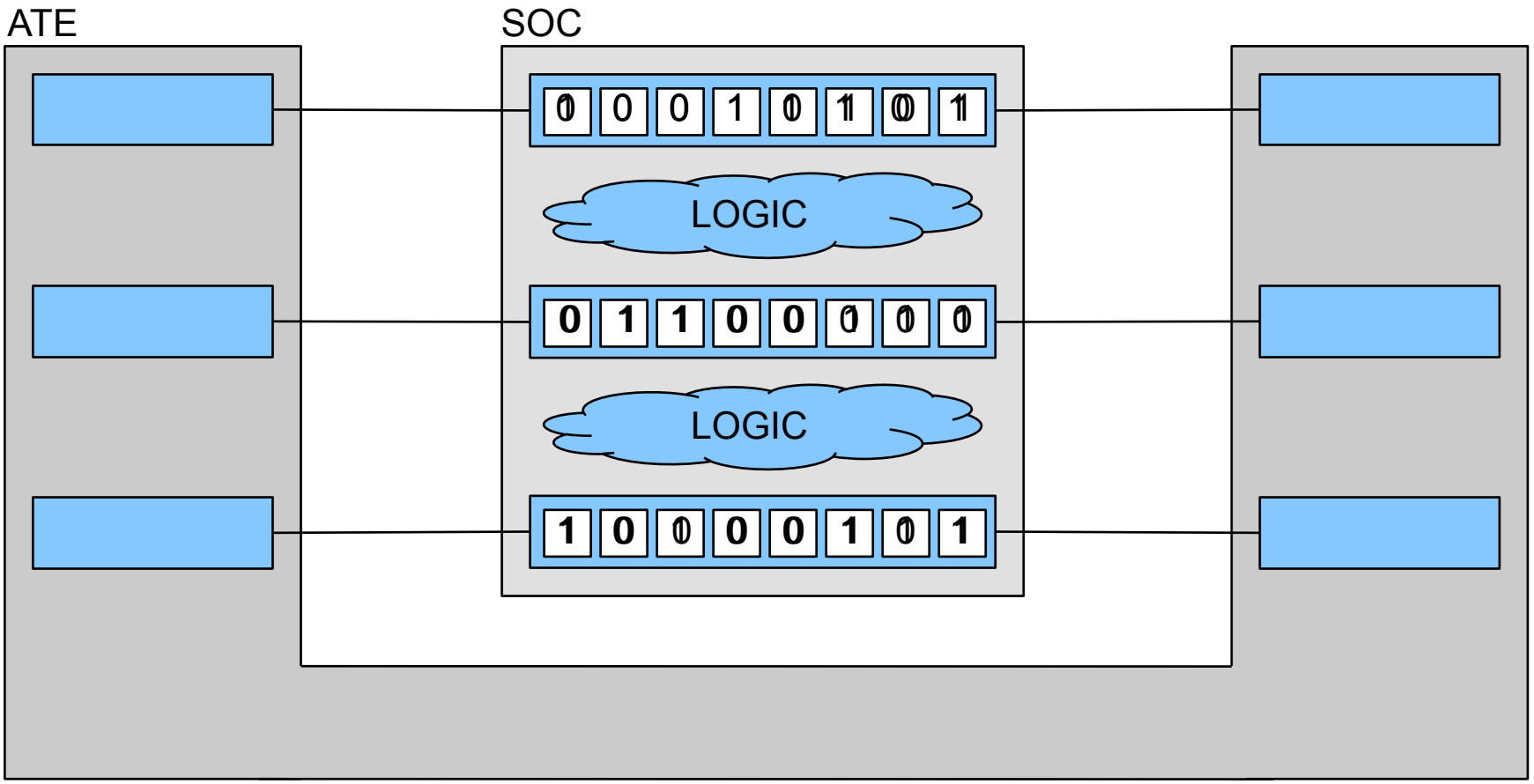
Capture Test Response



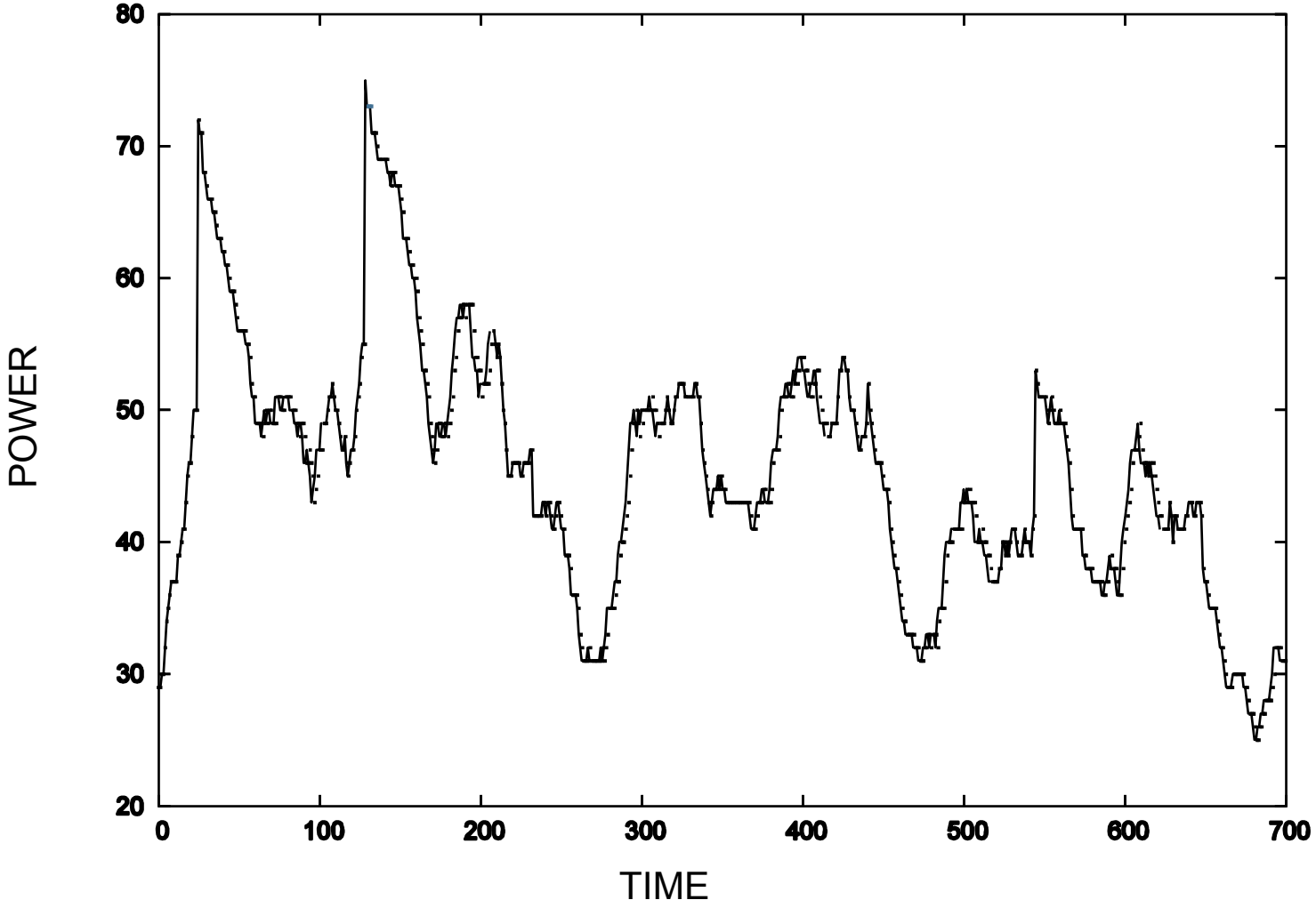
Test: Shift/Capture



Test: Shift/Capture

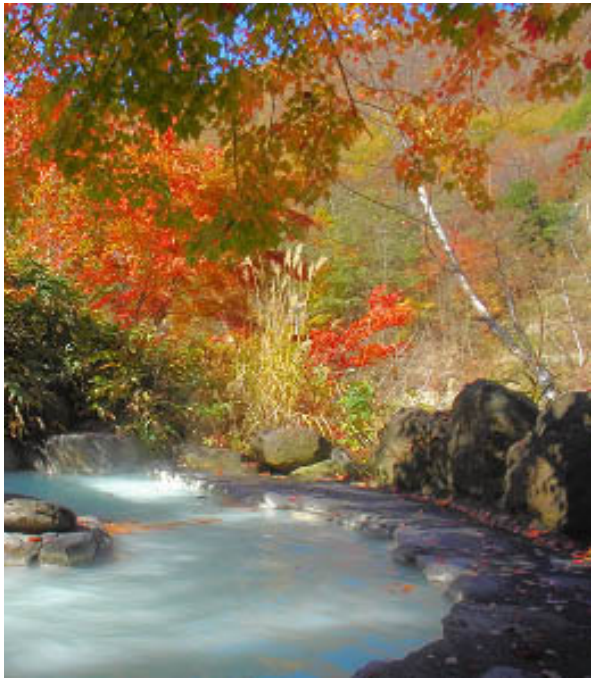


Power Consumption



Effect of Test Power Consumption

- Peak power consumption
- Average power consumption



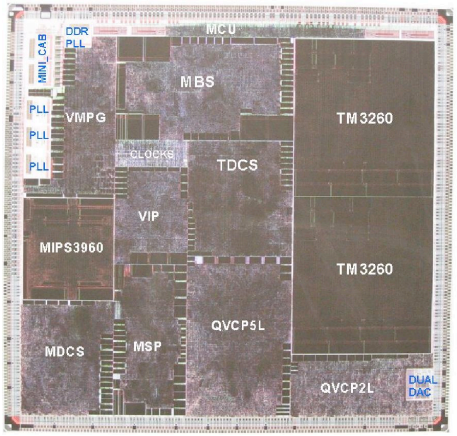
Power-Aware Test Approaches

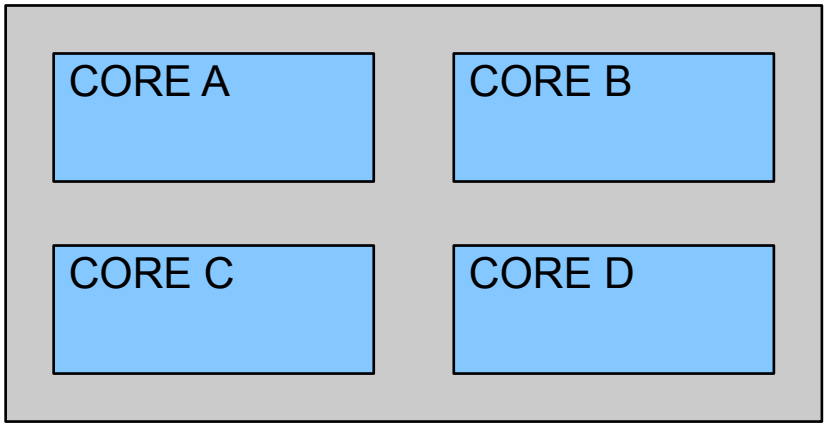
- Design SOC to handle test power consumption
- Design SOC with test power reducing techniques
- SOC test planning to handle test power consumption

- Test planning is a low-cost alternative to:
  - Explore ordering of tests to lower the test application time
  - Guide the search for bottlenecks where
    - design for low-power techniques are to be included or
    - (over) design for test power is needed

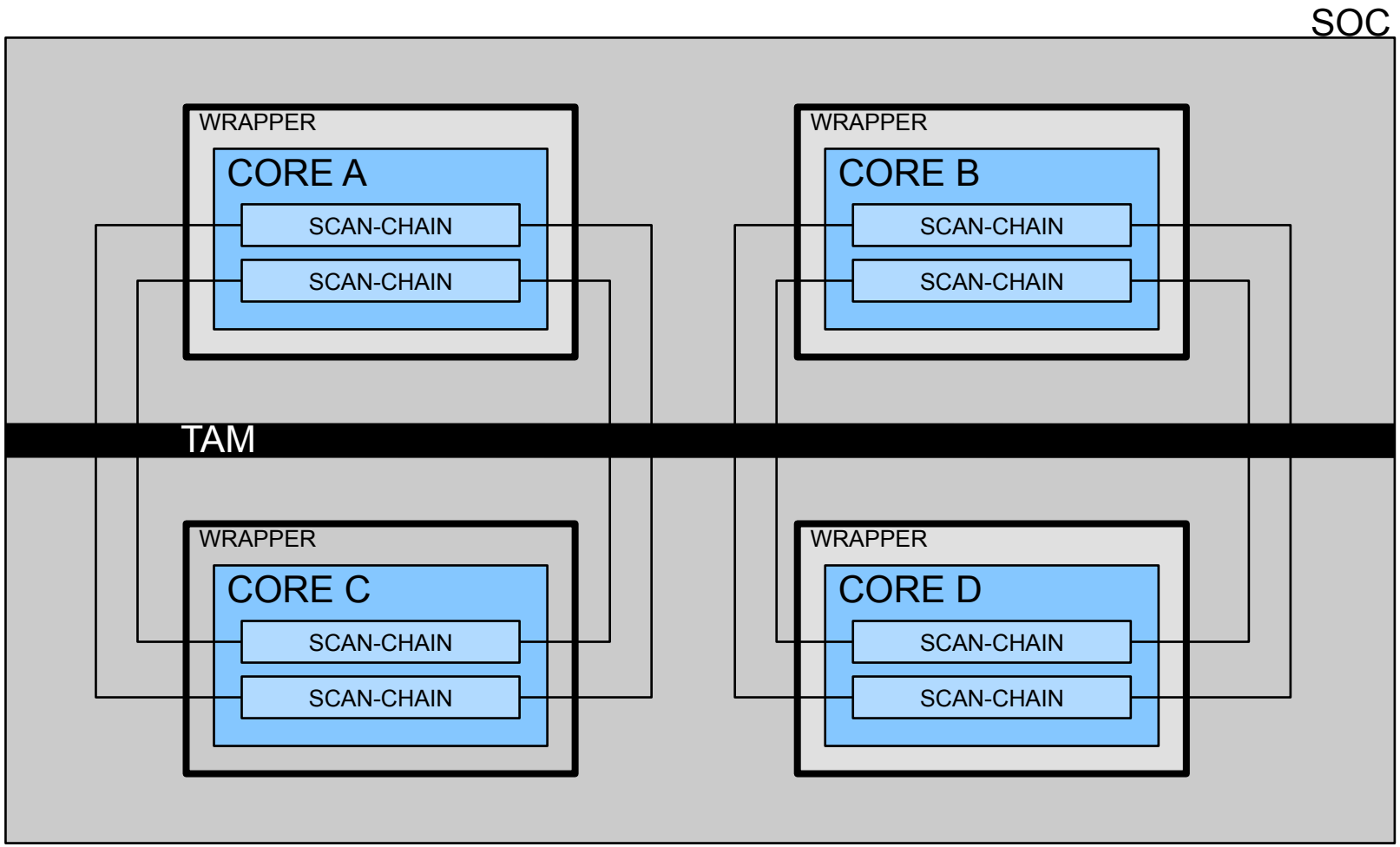
System-on-Chip

- Complete systems can be fabricated on single die
- Common to use pre-designed and pre-verified blocks of logic (cores); modular SOC.

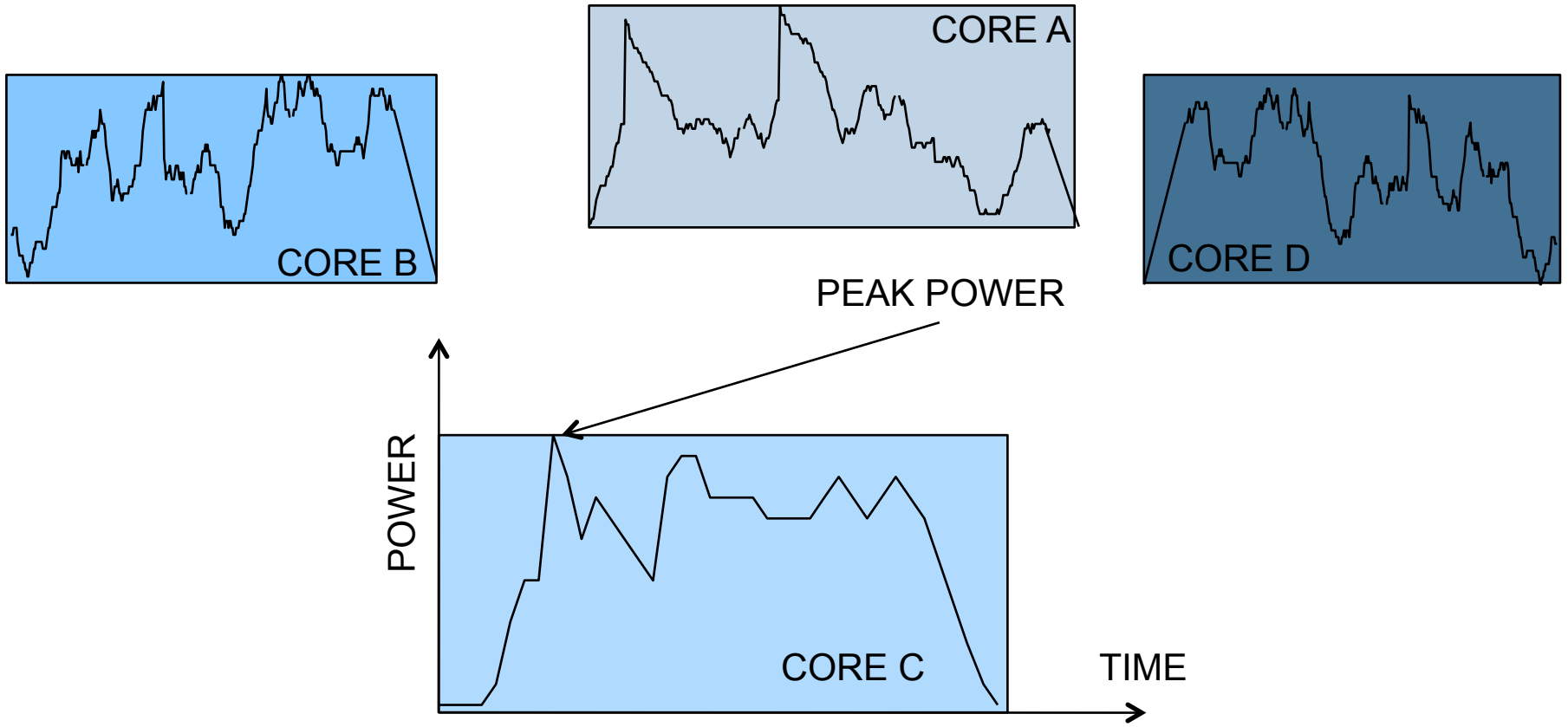




Modular Test of Core-based SOC

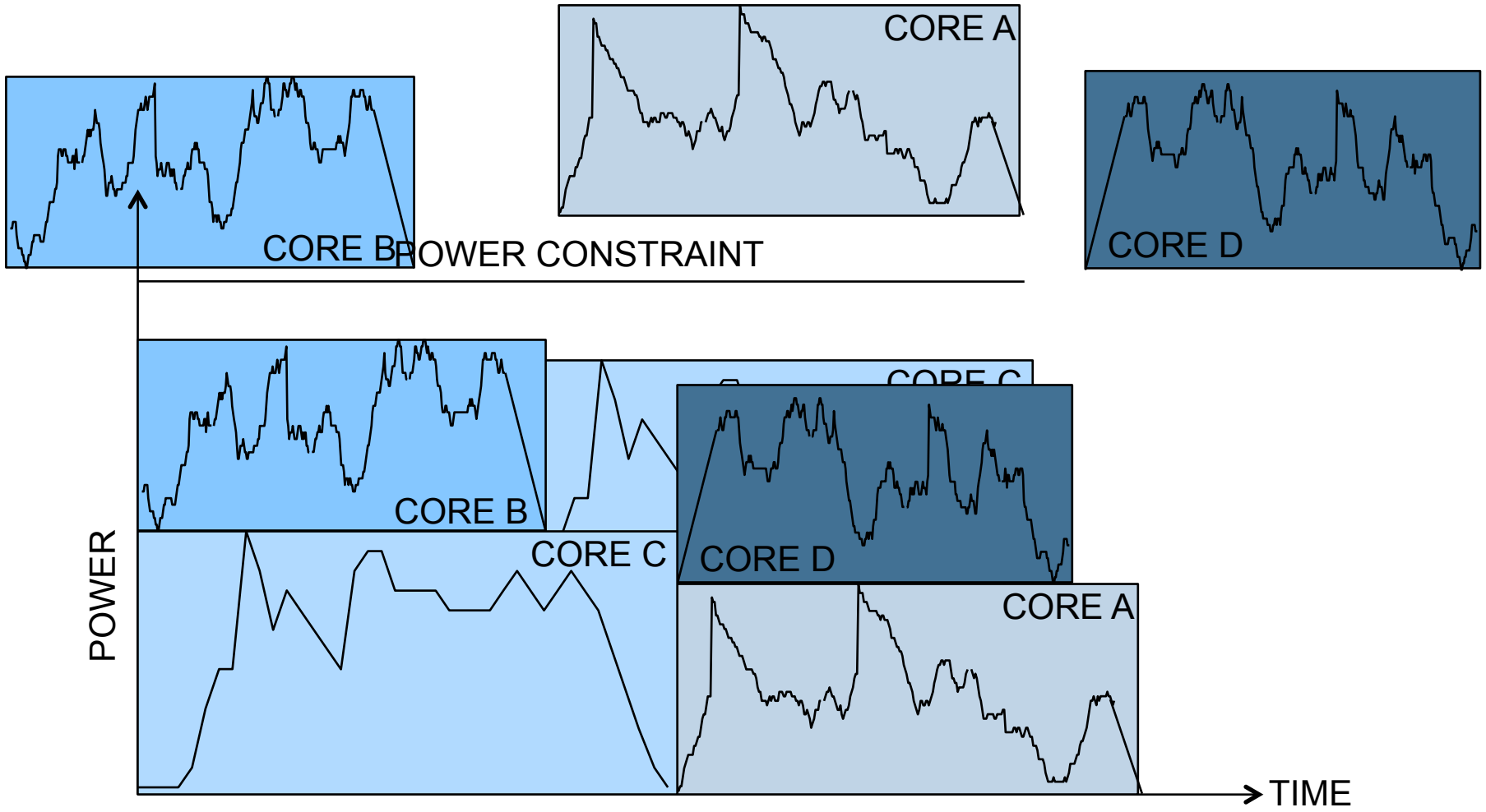


Peak-Power Model



Chou R. M., Saluja K. K., Agrawal V. D., “Scheduling tests for VLSI systems under power constraints”, IEEE transactions on very large scale integration (VLSI) systems, 1997, vol. 5, no2, pp. 175-185

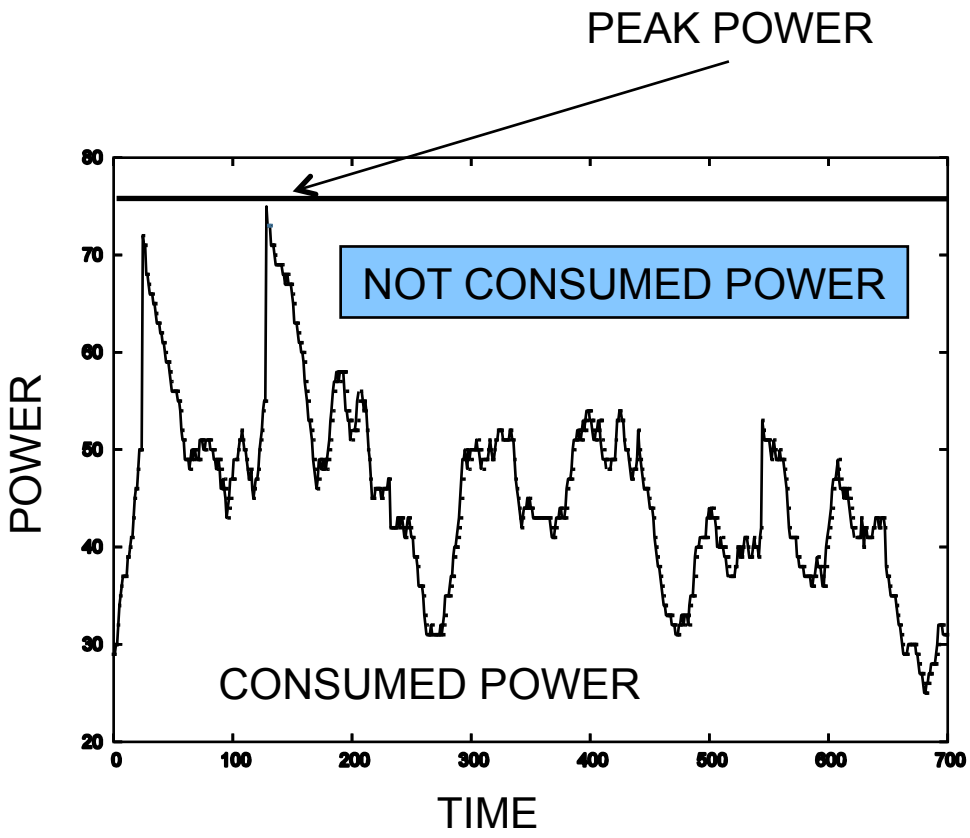
Power-Aware Test Planning



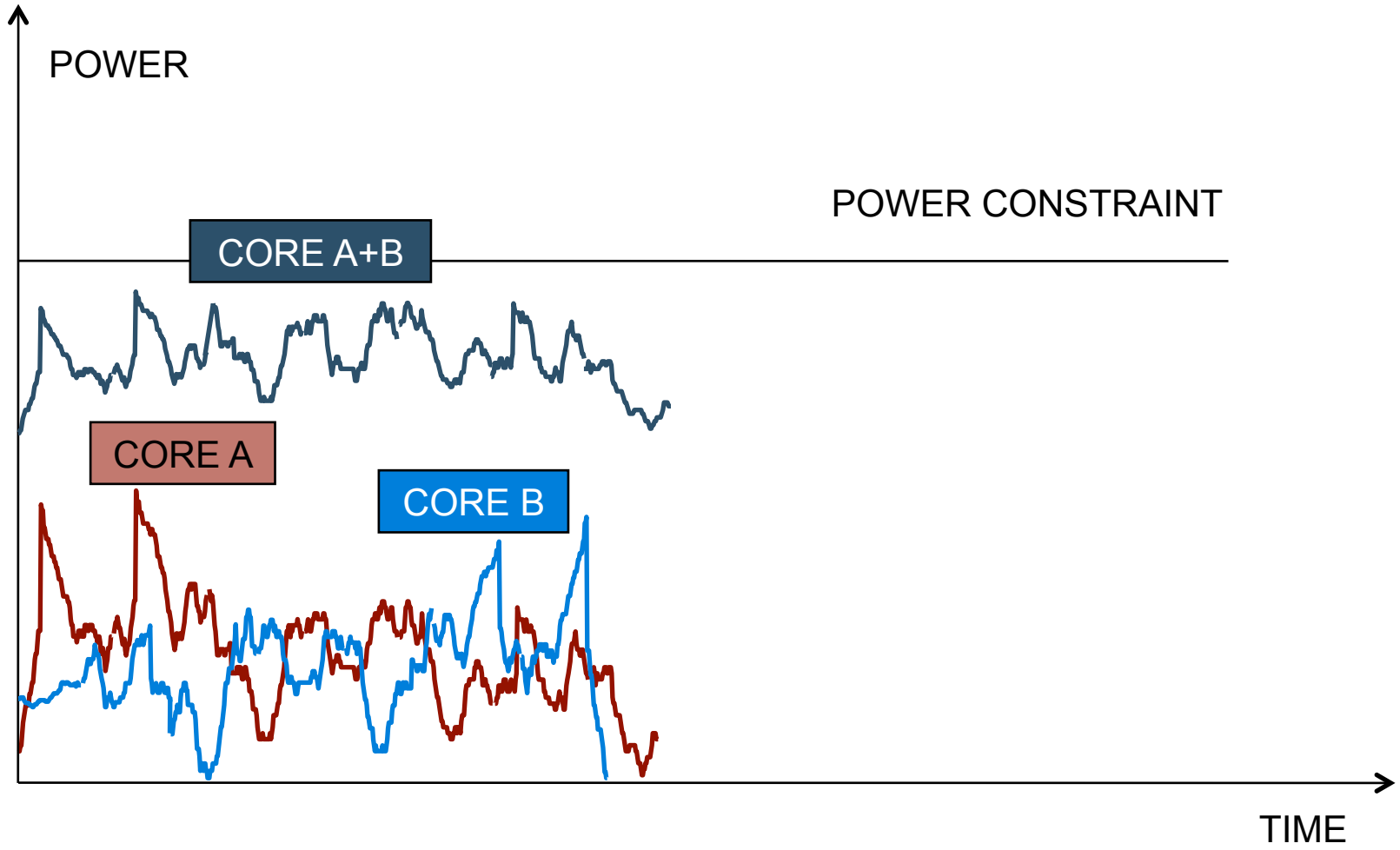
Chou R. M., Saluja K. K., Agrawal V. D., “Scheduling tests for VLSI systems under power constraints”, IEEE transactions on very large scale integration (VLSI) systems, 1997, vol. 5, no2, pp. 175-185

Global Peak-Power Model

- Advantage: Fast simulation
- Disadvantage:

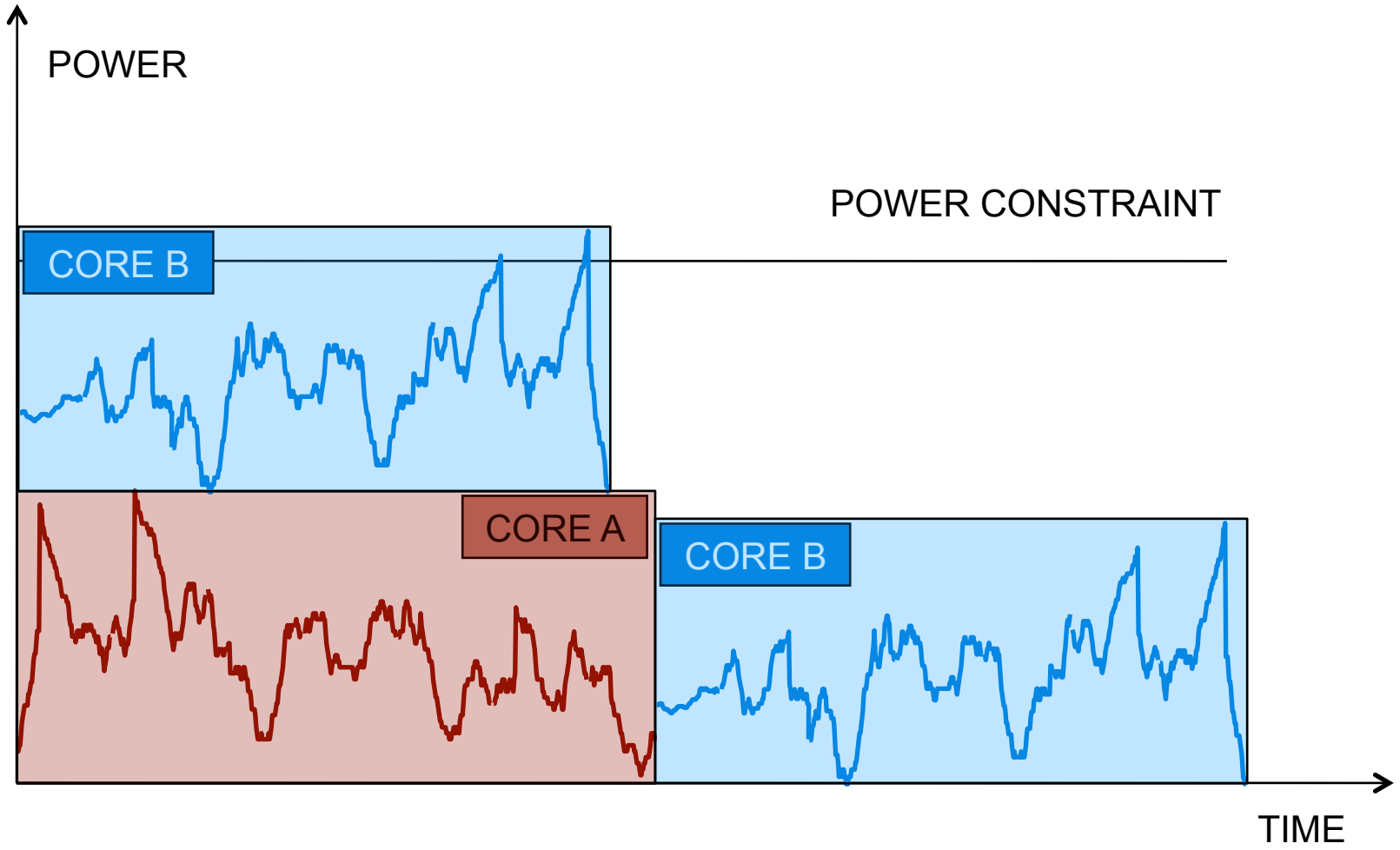


Global Peak-Power Model



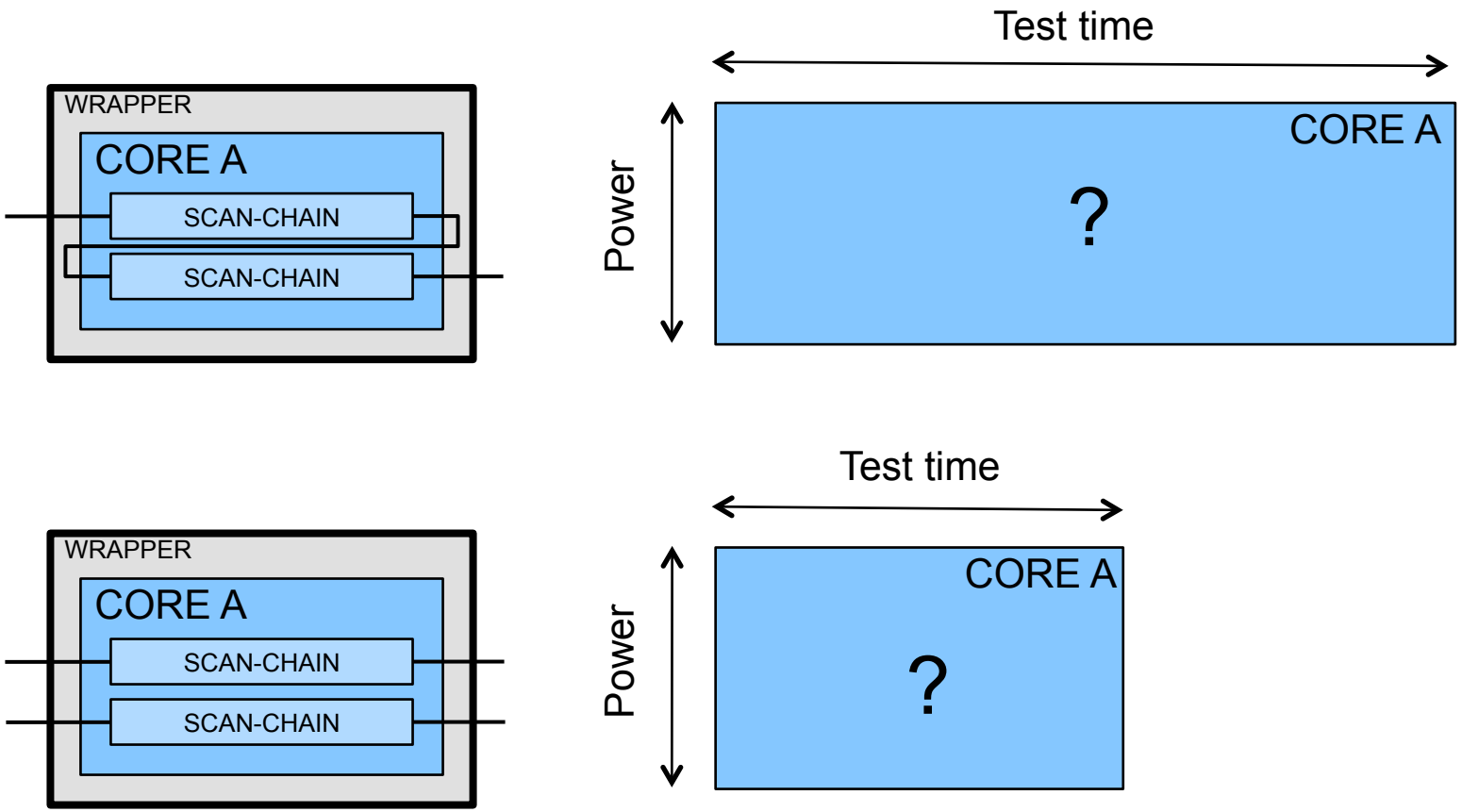
Samii, S.; Selkala, M.; Larsson, E.; Chakrabarty, K.; Zebo Peng, “Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977

Global Peak-Power Model



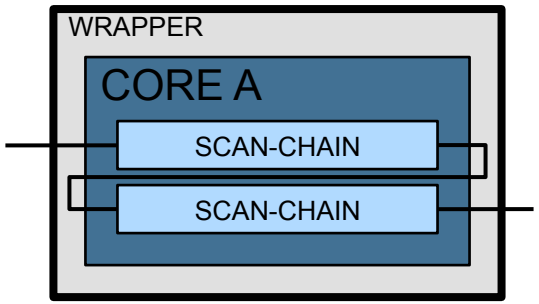
Samii, S.; Selkala, M.; Larsson, E.; Chakrabarty, K.; Zebo Peng, “Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977

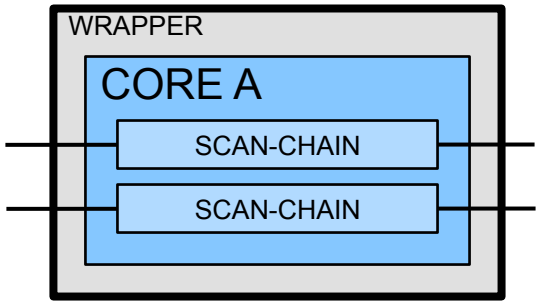
Power Profile and Wrapper Design

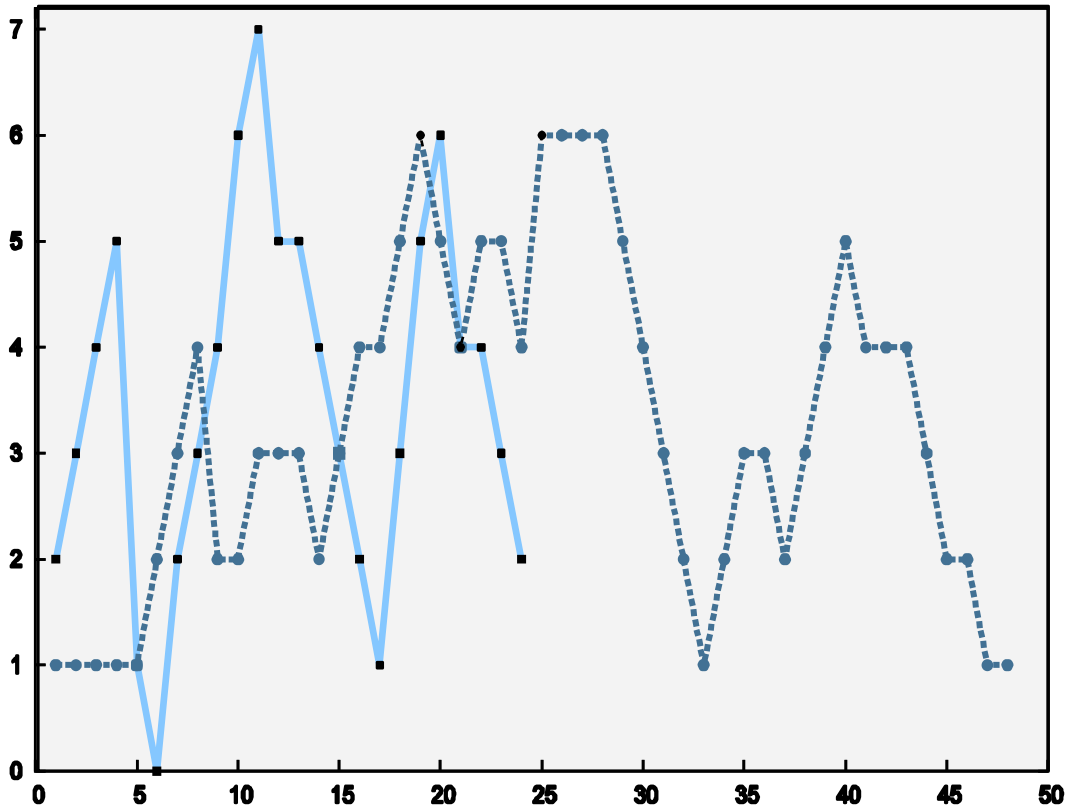


Samii, S.; Selkala, M.; Larsson, E.; Chakrabarty, K.; Zebo Peng, “Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977

Power Profile and Wrapper Design



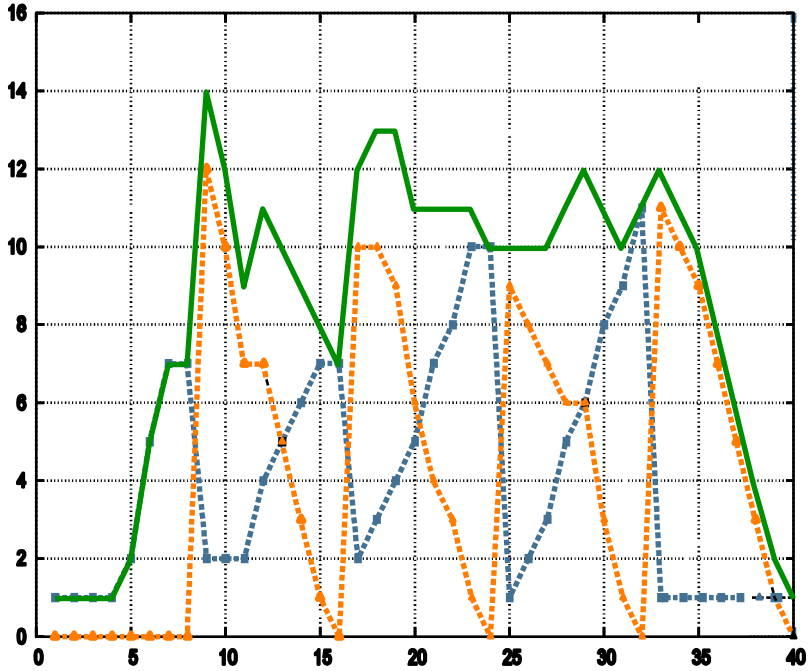




Samii, S.; Selkala, M.; Larsson, E.; Chakrabarty, K.; Zebo Peng, “Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977

Power Model

- Switch activity due to test stimuli and test responses shifting is highly related to IC's total power consumption, and
- Switch activity due to test stimuli shifting only is not related to IC's total power consumption



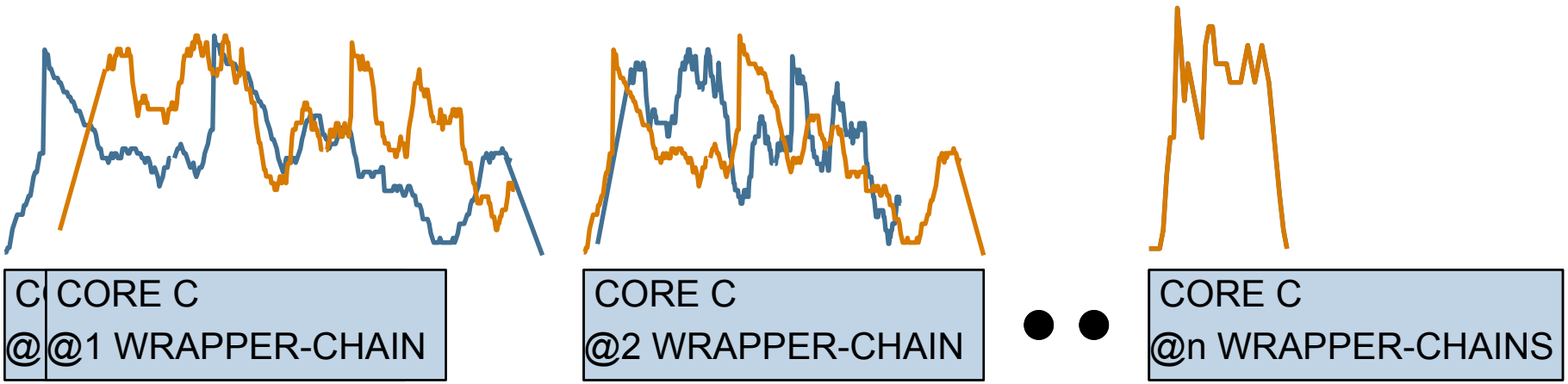
Total power

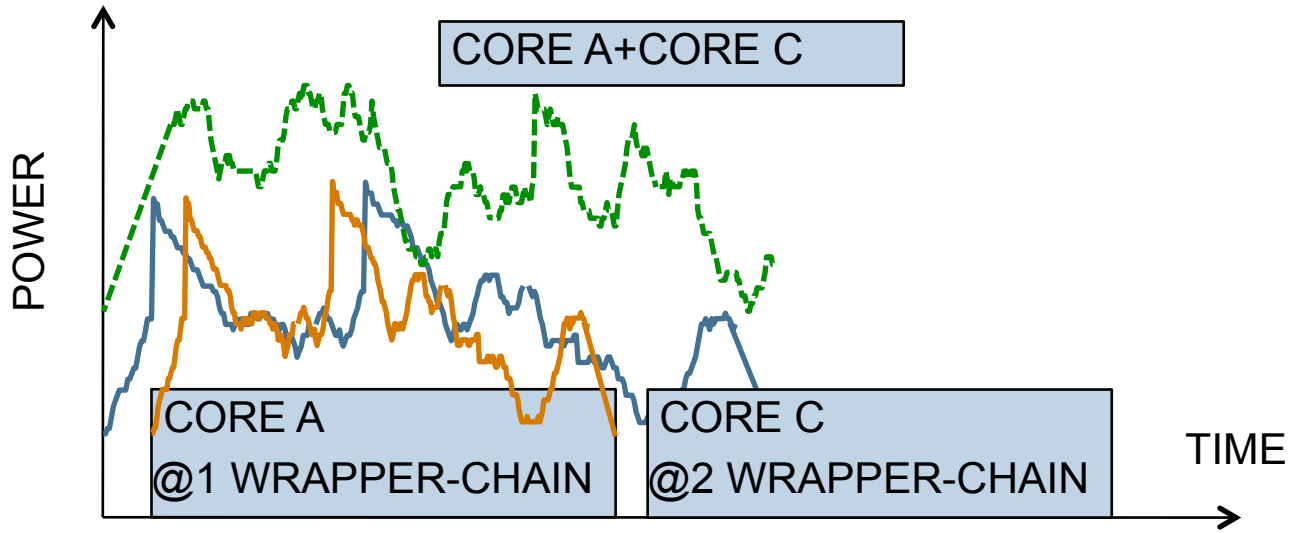
Power due to shift-in

Power due to shift-out

Samii, S.; Selkala, M.; Larsson, E.; Chakrabarty, K.; Zebo Peng, "Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977

Multi-Value Power Model



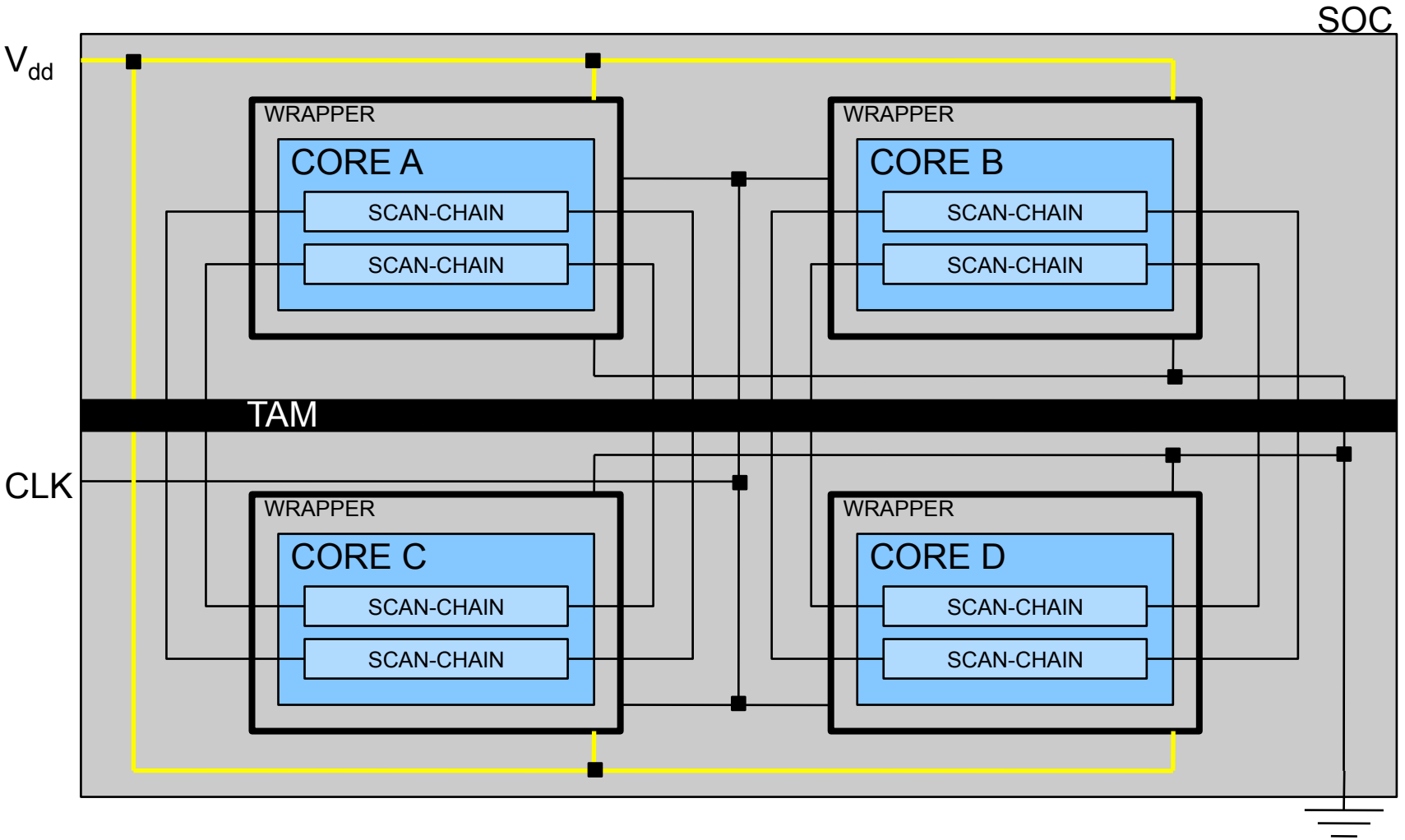


Samii, S.; Selkala, M.; Larsson, E.; Chakrabarty, K.; Zebo Peng, “Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 27, Issue 5, May 2008 Page(s):973 - 977

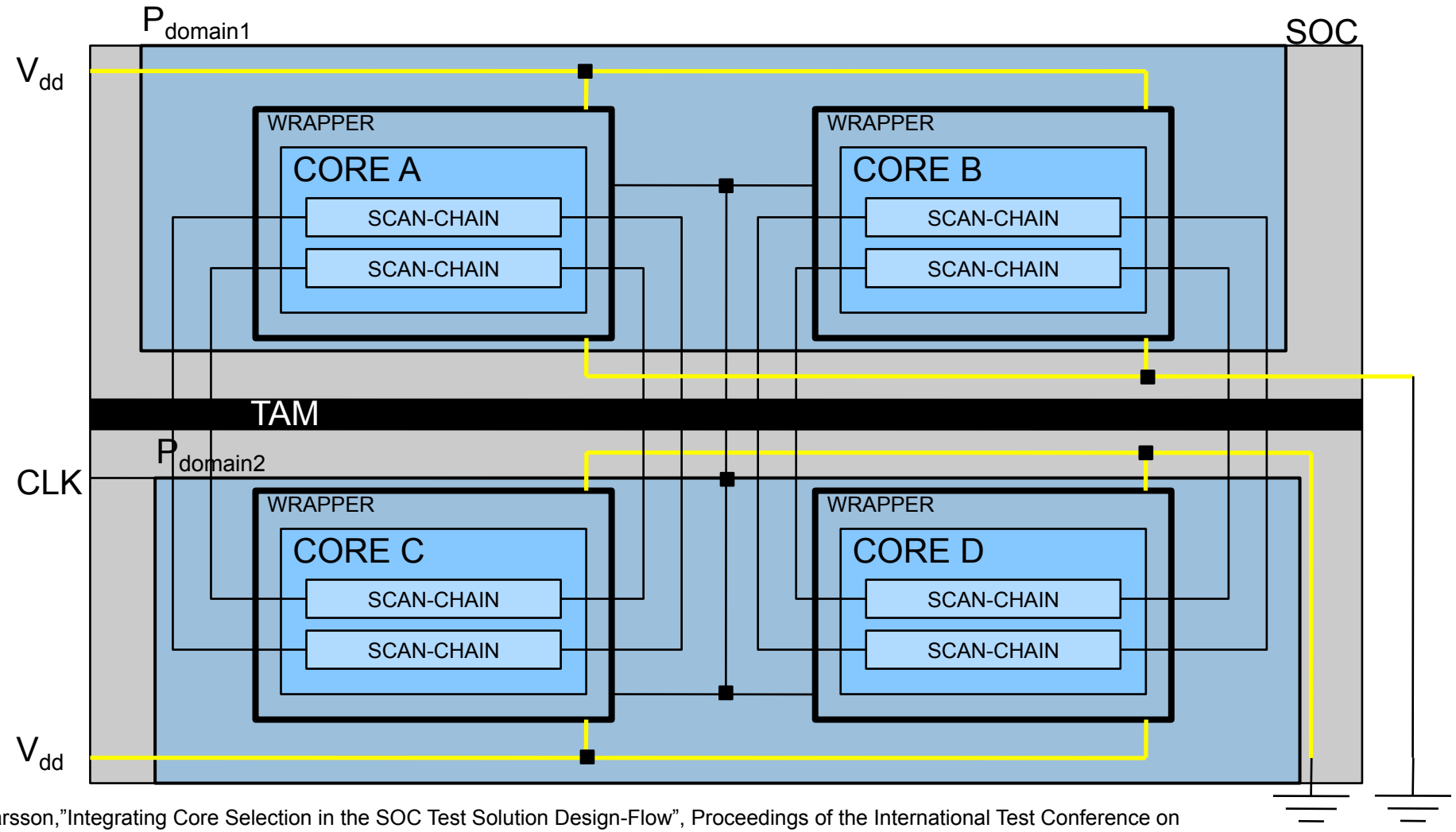
Power Modeling

- Power model:
  - single-value (peak-power model)
  - multiple-value (power profile)

Global Power Constrained Testing



Power-Grid Aware Test Planning



E. Larsson,"Integrating Core Selection in the SOC Test Solution Design-Flow", Proceedings of the International Test Conference on International Test Conference, 2004, pp.1349-1358

Power Constraints

- Power constraint:
  - single-value (single global power model)
  - multiple-value (power grid model)

Power Constraints and Power Modeling

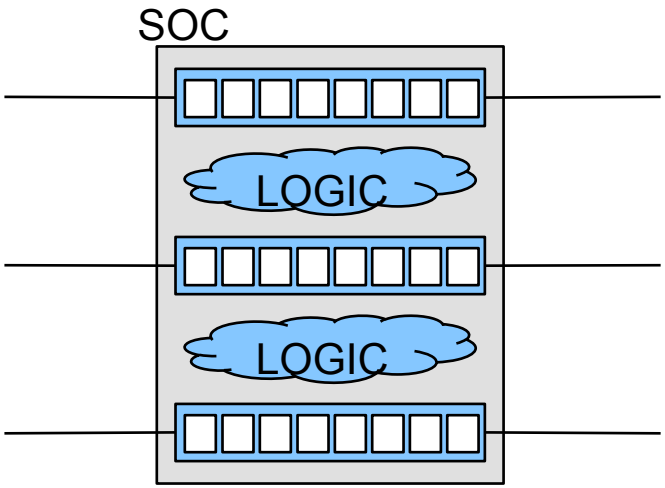
- Power model: single value or multiple value
- Power constraint: single value or multiple value

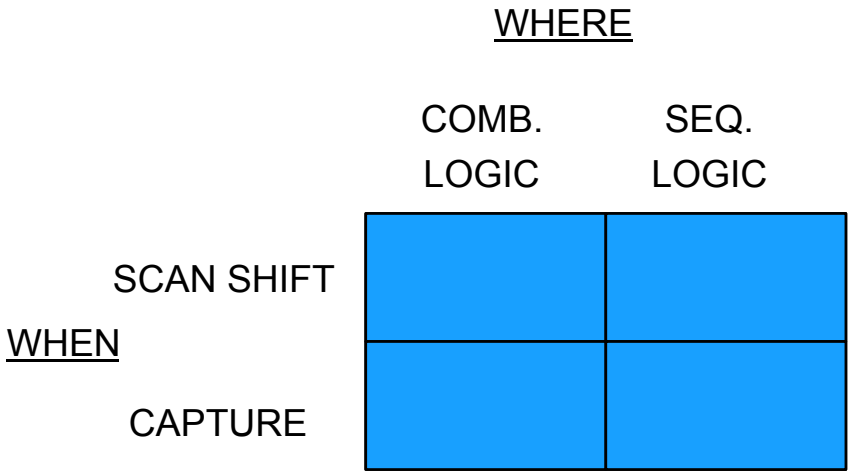
POWER MODEL	POWER CONSTRAINT: SINGLE-VALUE	POWER CONSTRAINT: MULTI-VALUE
SINGLE-VALUE	DONE	DONE
MULTI-VALUE	DONE	

Power-Aware Test Approaches

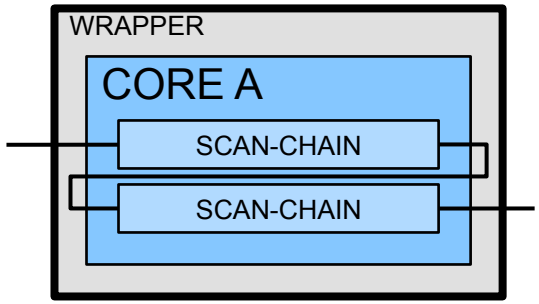
- Design to handle test power consumption
- Design with test power reducing techniques
- Plan testing to handle test power consumption

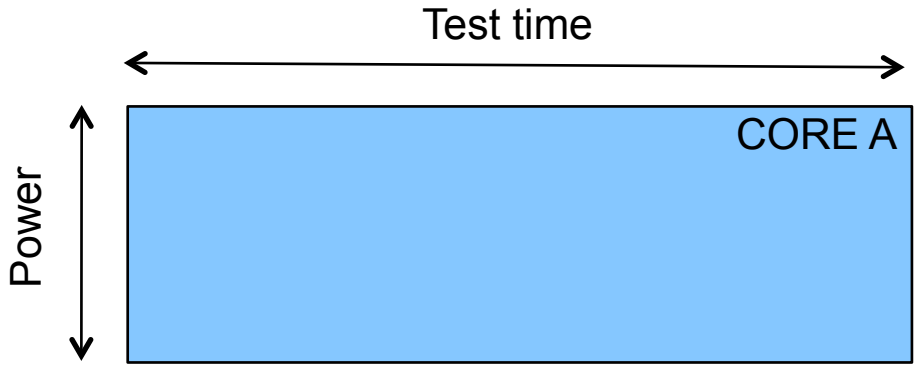
Test Power-Aware DfT



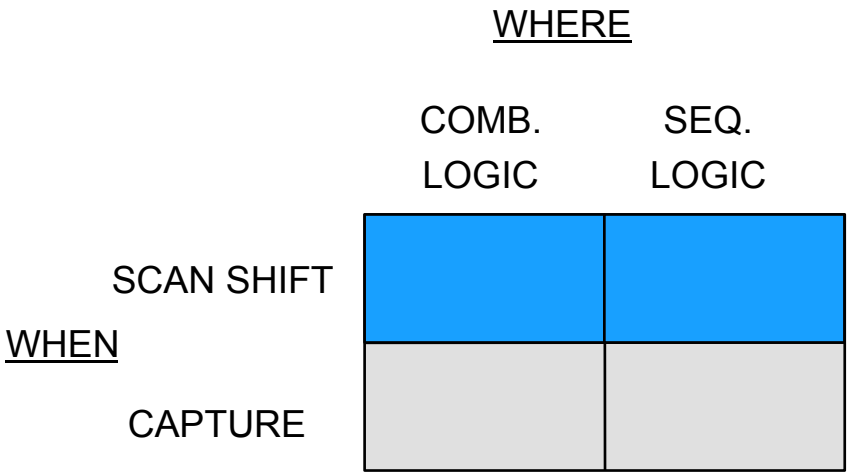


Clock-Gating

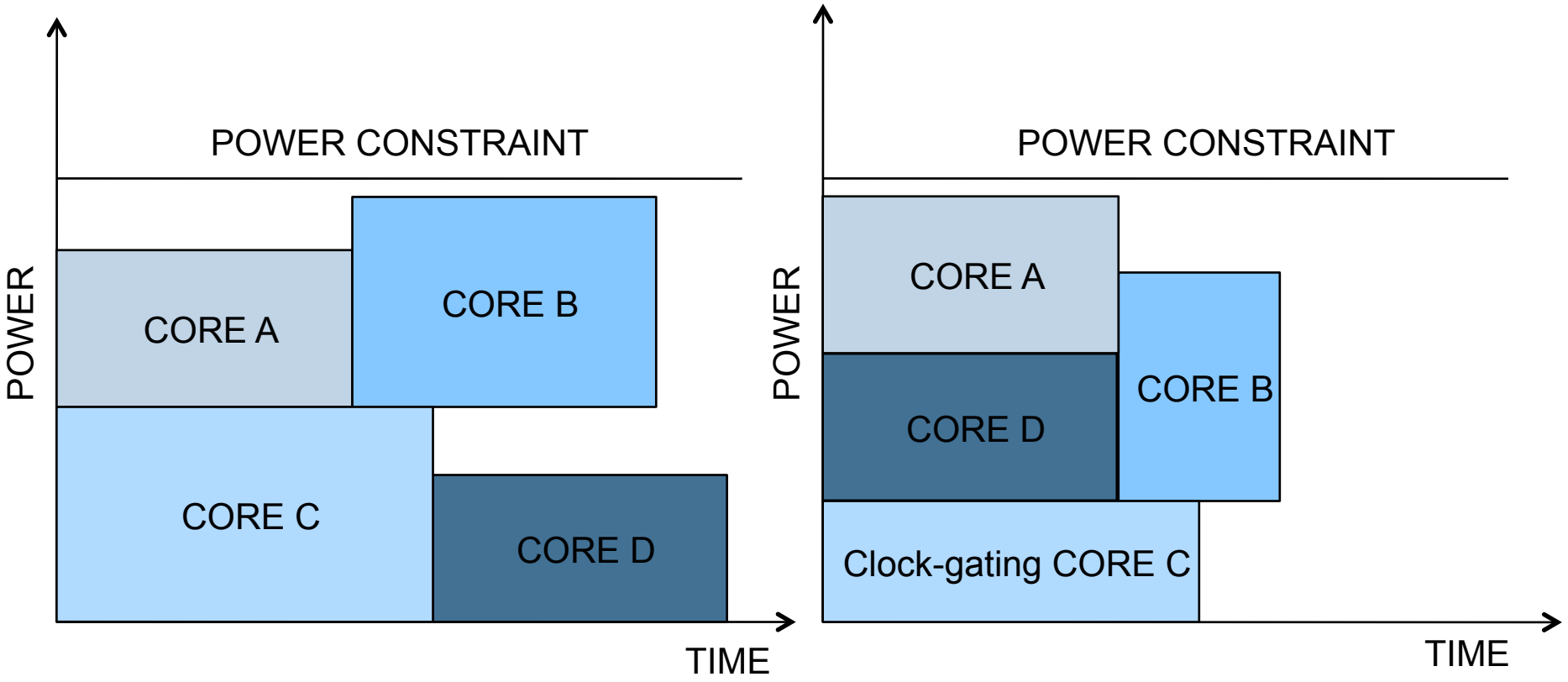




Clock-Gating



Test Planning with Power-Aware DfT



Larsson, E.; Arvidsson, K.; Fujiwara, H.; Zebo Peng, “Efficient test solutions for core-based designs”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 23, Issue 5, May 2004 Page(s): 758 - 775

Conclusion

- High power consumption during test is a problem
- Approaches:
  - Design to handle test power consumption
  - Design with test power reducing techniques
  - Power-aware test planning
- Test planning can be used to ex ng
  e manufac
- – combine test planning with:
  - Design with test power reducing techniques
  - Design to handle test power consumption

Computer engineers working with test

Electrical engineers working with test

Electrical engineers working with design

Future Directions

- To be or not to be?
  - Modular versus non-modular SOCs
  - Test planning versus no test planning
- And where is work needed?

Test Planning

POWER MODEL	POWER CONSTRAINT: SINGLE-VALUE	POWER CONSTRAINT: MULTI-VALUE
SINGLE-VALUE	MUCH WORK	SOME WORK
MULTI-VALUE	SOME WORK	LITTLE WORK

Test Planning+Power-Aware DfT

WHEN	WHERE: COMB. LOGIC	WHERE: SEQ. LOGIC
SCAN SHIFT	SOME WORK	SOME WORK
CAPTURE	LITTLE WORK	LITTLE WORK

Power-Aware System-on-Chip Test Planning

Erik Larsson

Department of Computer Science

Linköping University

Sweden

LiU expanding reality