CALL FOR PARTICIPATION

WRTLT'08

The Ninth IEEE Workshop on RTL and High Level Testing

Nov. 27-28, 2008 ACU (Advanced Center for Universities), Sapporo, Japan
(To be held in conjunction with ATS'08)

Sponsored by
IEEE Computer Society Test Technology Technical Council
IEICE-ISS, Technical Committee on Dependable Computing

Scope:
The purpose of this workshop is to bring researchers and practitioners on LSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing. Areas of interest include:
(1) High level Testing -- RTL/Behavior level testing, High level approaches for testing, RTL ATPG, RTL DFT, RTL BIST, Synthesis for testability, Relationship between RTL and gate level testing, Functional fault modeling, High level test bench generation
(2) SoC Testing -- Test scheduling, Core testing, Interconnect testing, NoC testing
(3) Reliable SoC -- System level reliability, Self repair, Fault tolerant SoC
(4) Micro Processor Testing (5) Design Verification
(6) Gate Level Test Related Issues -- Low power testing, Test compression, ATPG, DFT, BIST

Program Introduction:
This year we set up the theme of **"Power/Thermal-Aware Testing"**, which we believe needs to be discussed not only at gate level but also from high level in this workshop. The following keynote speech, invited talk, and panel discussion on this theme will be scheduled in the afternoon of the first day, November 27.

Keynote Speech: " **Power-Aware System-on-Chip Test Planning**"
by **Erik Larsson**, Linkoping University, Sweden

Invited Talk: " **Power: The New Dimension of Test** "
by **Patrick Girard**, LIRMM, France

Panel:: "**Roads to Power-Safe LSI Testing**"
Organizer: **K. Hatayama**, Semiconductor Technology Academic Research Center, Japan
Moderator: **X. Wen**, Kyushu Institute of Technology, Japan
Panelists: **M. Tehranipoor**, University of Connecticut, USA
S. Ravi, Texas Instruments India, Pvt. Ltd., India
K. Ishibashi, Renesas Technology Corp., Japan
K. Chakravadhanula, Cadence Design Systems, Inc. USA

Twenty three papers in the WRTLT'08 scope will be presented in regular sessions. The advance program is available on our web-site.

Registration:
Advance registration deadline: Oct. 24, 2008
The registration form is now available on our web-site.

WRTLT'08 web-site: http://aries3a.cse.kyutech.ac.jp/wrtlt08

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