



2014 International Symposium on Dependable Integrated Systems



March 10, 2014

Graduate Seminar Room 7F, General Research Building, Iizuka Campus, Kyutech
Dependable Integrated Systems Research Center
Kyushu Institute of Technology

■ 09:30~09:40: Opening & Introduction to DISC

Xiaoqing Wen, DISC, Kyutech, Japan

■ 09:40~10:30: Invited Talk 1

• **Using FPGAs in Automotive & Industrial Applications**

Brad Kadet, Altera, USA

■ 10:30~11:20: Invited Talk 2

• **Implementation of ATE Timing Circuits on FPGA**

Jiun-Lang Huang, National Taiwan University, Taiwan

■ 11:20~12:10: Invited Talk 3

• **Why I Started My Own Company at the Age of 29?**

- **My perspective on future work shift through my career of 6 years and in 3 countries -**

Shusei Hanibuchi, Capsule Inc., Japan

■ 12:10~13:20: Lunch

■ 13:20~15:00: DISC-Presentation-I

Chair: Stefan Holst, DISC, Kyutech, Japan

• **Algorithm and Hardware Design of a Quasi MLD Decoder for MIMO Systems**

Hong Trang Thi, Yuhei Nagao, Hiroshi Ochi

• **Hardware Implementation of a MIMO Channel Emulator**

Tran Thi Thao Nguyen, Leonardo Lanante, Yuhei Nagao, Hiroshi Ochi

• **High Definition Video Transmission System using Channel Characteristics**

Masafumi Ito, Koji Tashiro, Daiki Sakata, Masayuki Kurosaki, Hiroshi Ochi

• **Mosaic SRAM Cell TEGs with Intentionally-Added Device Variability for Confirming the Ratio-less SRAM Operation**

Hitoshi Okamura, Takahiko Saito, Hiroaki Goto, Masahiro Yamamoto, Kazuyuki Nakamura

■ 15:00~15:20: Break

■ 15:20~17:00: DISC-Presentation-II

Chair: Kohei Miyase, DISC, Kyutech, Japan

• **A Stabilization Technique for Intermediate Power Level in Stacked-Vdd ICs using Parallel I/O Signal Coding**

Naoya Kubo, Tomofumi Nishiyama, Taiki Koizuka, Hitoshi Okamura, Tomoyuki Yamanokuchi, Kazuyuki Nakamura

• **Test Power Reduction for Logic-BIST**

Senling Wang, Yasuo Sato, Seiji Kajihara, Kohei Miyase

• **A Temperature and Voltage Monitor for Field Test**

Yousuke Miyake, Yasuo Sato, Seiji Kajihara, Yukiya Miura

• **Study on X-Filling of Test Pattern for Low-Power Test**

Fuqiang Li, Kohei Miyase, Stefan Holst, Xiaoqing Wen

■ 17:00~17:05: Closing

Seiji Kajihara, DISC, Kyutech, Japan