

Title: Design-for-Test and Test of Digital VLSI Circuits

Abstract:

In the one-day tutorial we plan to cover various aspects of digital logic testing as well as give our perspective on the current state-of-the-art in digital VLSI design and test. We will introduce basic concepts in test as well as cover some advanced concepts. Our goal is to give background for the attendees who can pursue further studies in VLSI and/or pursue research and advanced academic studies, especially in test and design of digital VLSI circuits. The attendees need to have been exposed to digital logic design and introductory material on CMOS digital circuits.

Part I: Lectures by Prof. Sudhakar Reddy (University of Iowa, USA)

Topics:

- a. State of VLSI Industry and Employment Opportunities
- b. Introduction to Logic Testing
- c. Fault models, fault simulation, and ATPG
- d. Advanced topics -
 - i. Power-aware testing
 - ii. Generation of compact test sets
 - iii. Delay testing



Part II: Lectures by Dr. Nilanjan Mukherjee (Mentor Graphics, USA)

Topics:

- a. Basics of Test Compression
- b. Logic BIST and Hybrid EDT/LBIST Schemes
- c. Memory testing
- d. Advanced topics -
 - i. Delay test
 - ii. Cell-aware test
 - iii. Recent advances in test compression



当日のプログラム、会場、申し込みについて裏面に続きます

プログラム

10 : 00 ~ センター長挨拶・アナウンスなど

10 : 15 ~ 13 : 00 Part I: Prof. Reddy

- State of VLSI Industry and Employment Opportunities
- Introduction to Logic Testing
- Fault models, fault simulation, and ATPG
- Advanced topics
Power-aware testing, generation of compact test set, delay testing

13 : 00 ~ 14 : 15 昼食

(各自でお願い致します。混雑時を避けて少し長めにしています)

14 : 15 ~ 17 : 00 Part II: Dr. Mukherjee

- Basics of Test Compression
- Logic BIST and hybrid EDT/LBIST schemes
- Memory testing
- Advanced topics
Delay test, cell-aware test, recent advances in test compression

17:00 ~ 18 : 30 LSIテストに関する討論会

(詳細につきましてはお申込み頂いた皆様にご個別にご連絡致します)

セミナー会場

会場名：電気ビル共創館（会議室は、共創館の会場案内等でお知らせ致します）

所在地：福岡市中央区渡辺通2丁目1番82号

TEL : 092-781-0685

本セミナーへの申し込み・お問い合わせ先

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主催：
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研究センター

