2018 International Symposium on Dependable Integrated Systems

January 22, 2018
Graduate Seminar Room 7F, General Research Building, Iizuka Campus
Dependable Integrated Systems Research Center, Kyushu Institute of Technology

09:30–09:35  Opening Remarks
Seiji Kajihara, Dean of School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Japan

09:35–09:40  Introduction to DISC
Hiroshi Ochi, Professor and Director of DISC, Kyushu Institute of Technology, Japan

09:40–11:10  Keynote/Tutorial
• Has Fault Model Based Structural Test Hit a Brick Wall? Are In-System Tests Unavoidable?
  Adit Singh, James B. Davis Professor, Dept. of Electrical and Computer Engineering, Auburn University, USA

11:10–11:30  Break

11:30–12:00  Invited Talk
• Interval Property Checking for Hardware Design Using Satisfiability Modulo Theories Solver
  Nguyen Duc Minh, Professor, School of Electronics and Telecommunications, Hanoi University of Science and Technology, Vietnam

12:00–13:00  Lunch

13:00–14:40  DISC Research Presentation I (LSI Design)
Chair: Leonardo Lanante, Assistant Professor, DISC, Kyushu Institute of Technology, Japan
1. A Multimode FFT Improvement for IEEE 802.11 ax WLAN Devices
  P. T.K. Dinh, L.T. Dinh, H. V. Tran, C.M. Duong, L. Lanante Jr, M. Kurosaki, M. D. Nguyen, and H. Ochi
2. Study of Neural Networks Implementation in FPGA using SW/HW Co-design
  N. b. Ismail, Y. Igarashi, M. Kurosaki, L. Lanante Jr, and H. Ochi
3. World's First Industrial Wireless LAN with Low Latency, High Reliability and Highly Safe
4. Fully Digital Ternary Content Addressable Memory using Ratio-less SRAM Cells and Hierarchical-AND Matching Comparator for Ultra-low-voltage Operation

14:40–15:00  Break

15:00–16:40  DISC Research Presentation II (LSI Test)
Chair: Kohei Miyase, Associate Professor, DISC, Kyushu Institute of Technology, Japan
5. Locating Hotspots with Justification Techniques in a Layout Design
  Y. Kawano, K. Miyase, X. Wen, and S. Kajihara
6. Flip-Flop Selection for Multi-Cycle Test with Partial Observation in Scan-Based Logic BIST
  S. Oshima, T. Kato, S. Wang, Y. Sato, and S. Kajihara
7. Good Die Prediction Modeling from Specific Results of Wafer Tests
  T. Nishimi, S. Kajihara, and Y. Nakamura
8. On Avoiding Test Data Corruption by Optimal Scan Chain Grouping
  Y. Zhang, S. Holst, X. Wen, K. Miyase, S. Kajihara, and J. Qian

16:40–16:45  Closing Remarks
Kazuyuki Nakamura, Professor, Center for Microelectronic System, Kyushu Institute of Technology, Japan

All presentation files can be downloaded from 2018/1/19 through the following link:
https://www.dropbox.com/s/mqs33fpq2b5zpbs/DISC-2018_Presentation_Files.zip?dl=0