Kyutech
Kyushu Institute of Technology

第2回
テストスプリングセミナーのご案内

DiSC International

2015年3月17日（火）：電気ビル共創館（福岡市天神地区）

Title: Design-for-Test and Test of Digital VLSI Circuits

Abstract:
In the one-day tutorial we plan to cover various aspects of digital logic testing as well as give our perspective on the current state-of-the-art in digital VLSI design and test. We will introduce basic concepts in test as well as cover some advanced concepts. Our goal is to give background for the attendees who can pursue further studies in VLSI and/or pursue research and advanced academic studies, especially in test and design of digital VLSI circuits. The attendees need to have been exposed to digital logic design and introductory material on CMOS digital circuits.

Part I: Lectures by Prof. Sudhakar Reddy (University of Iowa, USA)

Topics:

a. State of VLSI Industry and Employment Opportunities
b. Introduction to Logic Testing
c. Fault models, fault simulation, and ATPG
d. Advanced topics -
    i. Power-aware testing
    ii. Generation of compact test sets
    iii. Delay testing

Part II: Lectures by Dr. Nilanjan Mukherjee (Mentor Graphics, USA)

Topics:

a. Basics of Test Compression
b. Logic BIST and Hybrid EDT/LBIST Schemes
c. Memory testing
d. Advanced topics –
    i. Delay test
    ii. Cell-aware test
    iii. Recent advances in test compression

↓↓↓　当日のプログラム、会場、申し込みについて裏面に続きます