Power-Aware Testing

The Next Stage

Xiaoqing Wen
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High Functionality \rightarrow \text{Successful LSI Product} \rightarrow \text{Low Power}

Function-Mode

- Call
- Cam
- Web
- Mail

Low Functional Power
(Wide Use of PMS)

Test-Mode

- Call
- Cam
- Web
- Mail

High Test Power
(Needs to Handle PMS)

Growing Power Gap

Excessive Heat • Timing Failures
Higher Test Complexity due to PMS

Test Crisis
(Damage / Low Yield / High Cost)

Low Power Design

Power Aware Test

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Power-Aware Testing

Low-Power Test

Coarse-Grained

Unfocused (Global) Reduction
No Test Power Safety Guarantee
Risk of Over-Reduction
Power Reduction Only
Risk of Test Quality Degradation
Severe Test Data Inflation

Right-Power Test

Fine-Grained

Focused (Local) Reduction
Guaranteed Test Power Safety
No Over-Reduction
Possible Power Increase
Minimum Test Quality Impact
Minimum Test Data Inflation
Outline

1. Power: Excitement for Design Engineers
2. Power: Headach for Test Engineers
3. Test Power Analysis
4. Test Power Reduction
5. Next Stage and New Opportunities
Outline

1. Power: Excitement for Design Engineers
2. Power: Headache for Test Engineers
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5. Next Stage and New Opportunities
Design Engineers Love to Reduce Power

Avoid unnecessary operations
Clock Gating
Power Gating

and avoid unnecessary operation conditions
Multiple Supply Voltages (MSV)
Dynamic Voltage Frequency Scaling (DVFS)
Multiple Threshold Voltages (MTV)

by using power management structures.

Clock Gator
Power Switch
State Retention Register
Level Shifter
Isolation Cell
Power Management Controller

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Conventional Design

VDD
Low-Power Design

Power Management Structures

Power Domain 1
(Conditionally ON)

Power Domain 2
(Always ON)

Power Domain 3
(Always ON)

Power Control Logic

Power Switch

State Retention Register

Clock Gator

Isolation Cell

Enabled Level Shifter

Level Shifter

stop_clock / save / restore

iso_enable

ack

reg

ack

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1. Power: Excitement for Design Engineers
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Widening Function-Test Power Gap

Causing Problems Only During Test

Excessive Heat • Timing Failures

Power Management
(Hardware)
(Software)

Function-Test Power Gap

Excessive Test Power

Stronger Switching Activity in Test Mode

Parallelism (faults / blocks)

Non-Functional Test Data

Non-Functional Test Clocking

Test Time / Cost Constraints

Functional Power
(Conventional Design)

Functional Power
(Low-Power Design)

Test Power

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Impact of Test Power in At-Speed Scan Test (LOC)

Shift

Test Vector Load Started

Test Vector Load Completed

Capture

Launch Capture

Response Capture

SE

Many Shift Pulses

CLK

S₁

Sₗ

C₁

C₂

Shift Power

Scan Chain Failure

Capture Power

Capture Failure

Excessive Heat

Chip Damage

Reduced Reliability

High Test Cost

Yield Loss

(IR-Drop / L di/dt) - Induced Clock Skew & Delay Increase

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Power Management Structures Add to Test Complexity

Power Management Structures (PMS)

PMS-Specific DFT Solutions

PMS-Specific Test Generation

PMS-Aware Scan Design

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In the Old Days ...

- Scan Design
- Test Compression / BIST
- Testability Enhancement with TPI

Nowadays ...

- MSV-Aware Scan Design / Clock-Gating-Aware Scan Design
- Low-Power Test Compression / Low-Power BIST
- Testability Enhancement with TPI and for PMS (especially, power switches)
- Design for Shift Power Reduction / Design for Capture Power Reduction
Headache for Test Engineers ~ Reason 2 ~

Prepare Test Data

In the Old Days ...
- Conventional ATPG

Nowadays ...

Scan Test Power Reduction
- Test Power Analysis
- Test Power Reduction (low-shift-power ATPG / low-capture-power ATPG)

Power-Management-Specific Concerns
- System-Level Power-Aware Scheduling due to Limited Power Budget
- Test Generation for MSV
- Test Generation for Power Management Structures

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An Example: DFT for a Complex Power Switch

Micro Power Switch Chain for containing rush current

Micro Power Switch Chain with test wrapper implementation

One Power Switch before DFT

One Power Switch after DFT

Basic Tasks in Handling Function-Test Power Gap

- Test Power Analysis
- Test Power Reduction

Functional Power
Test Power (without power-aware test)
Test Power (with power-aware test)
Outline

➊ Power: Excitement for Design Engineers

➋ Power: Headach for Test Engineers

➌ Test Power Analysis

➍ Test Power Reduction

➎ Next Stage and New Opportunities
Ideal vs. Reality

Switching Activity

- Accurate but costly.
- OK for sign-off but bad for use in DFT/ATPG.

- Fast and accurate-enough approximation needed.
- Gate-level metric preferred.

Temp. Analysis, IR-Drop Analysis + Delay Analysis, Sensitization Analysis

Excessive Heat, Excessive Delay along Sensitized Paths
Global Analysis

Shift Power

Weighted_Transitions = \sum (Scan\_Chain\_Length - Transition\_Position)

Global Analysis

Capture Power

Toggle Count
\[ \sum \text{transitions with weight of 1} \]

Weighted Switching Activity (WSA)
\[ \sum \text{transitions with weight of fanout (+1)} \]

B19 ITC'99 Benchmark (196K Gates)

160 Test Vectors \[ \rightarrow \] WSAave = 47.7%

Risky Test Vectors: Ta, Tb \[ \rightarrow \] WSA(Ta) = 44.8% / WSA(Tb) = 46.7%
Use the WSA of the Impact Area of P to determine if P may have timing failure.

Capture Power

Local Analysis

Impact Area of Path P  
On-Path Gate G

Aggressor Region of Gate G

Long Sensitized Path P

Target Gate  
Powering Via

M2  
M3  
M3  
M3

Aggressors

M2

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Basic Strategies

Shift Power Reduction

Capture Power Reduction
Basic Strategies
Different Characteristics of Shift and Capture Power

Shift

Capture

Many Shift Pulses

Fast Test Cycle

Characteristics

Shift Power ≠ Capture Power

Different Reduction Strategies Needed
Characteristics of Shift Power

- Shifting a test vector often causes heavy switching.
- IR-drop may be worse in shift mode than in capture mode.
- All test vectors contribute to the shift power problem.
- Slowing down helps reduce heat impact but not clock skew.
- Circuit / clock change has no impact on ATPG, time, size, and FC.
- Only scan chains need to be considered as sensitized paths.
Timing Failure due to excessive delay increase along long sensitized paths.

Capture power mostly impacts sensitized paths.

Reducing capture power may be needed to avoid yield loss.

Circuit / clock change may impact ATPG, time, size, and FC.

Capture power depends on the content of a test vector.

A small portion of test vectors suffers from excessive capture power.

Increasing capture power may help to improve test quality.

Power management circuitry helps reduce capture power.
Basic Strategies for Test Power Reduction (except BIST)

Type of Test Power Reduction Techniques

- **Soft**: Test Data Manipulation
- **Hard**: Circuit Modification

Effect

- **Soft—Soft**:
  - Shift Power Reduction
  - Capture Power Reduction

- **Hard—Soft**:
  - Shift Power Reduction
  - Capture Power Reduction

- **Hard—Soft**:
  - Predictable effect of shift power reduction
  - More test data for capture power reduction

Overhead
Shift Power Reduction

- Excessive Heat
- Shift Power
- Scan Chain Failure

- Test Vector Load Started
- Test Vector Load Completed

- SE
- CK
- S₁
- Sᴸ
Scan Segmentation

Predictable and data-independent shift (in & out) power reduction.
No change to ATPG and no increase in test application time.

Capture Power Reduction
Basic Idea

Minimize the Hamming Distance between PPI and PPO

Vector

Combinational Portion
Capture Switching Activity

Response

PPI

0 1 0
FF1 FF2 FF3

PPO

0 1 0

IR-Drop

Delay Increase

Timing

Malfunction
(Test-Induced Yield Loss)
Basic Approaches

Reduce the Number of Simultaneously-Capturing FFs

Clock Control Modification

Stop the Clock

Test Vector Manipulation

In-ATPG / Post-ATPG
(Gated Clock Disabling)

Equalize D and Q

Test Vector Manipulation

In-ATPG
(Constraint-Based ATPG)
Post-ATPG
(Low-Capture-Power X-Filling)
An Example: Processing Flow

Assign logic values for X-bits so that PPI = PPO.

Easy to implement. No or little test data increase.
An Example: Evaluation Results

Industrial Circuit
(90nm process / 1.2V / 50K gates / 2.5% VDD IR-drop budget)

Chip-Level IR-Drop Distribution

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Ultimate Goals in Power-Aware Testing

- Uncompromised Test Quality
- Guaranteed Test Power Safety
- Minimized Test Cost Impact

Test Quality and Test Power are connected by a trade-off, while Test Cost is preserved.
Current Problems
**Problem:** Lack of Information on Test Power Impact

- Which test vector is power-risky?
- Which part of the chip suffers from excessive test power?

**Local Test Power Analysis Needed**
Problem: Clock Skew during Scan Shift

Excessive Heat → Good Solutions

Combination Portion

Clock Tree

Excessive Clock Skew

Local Shift Power Management Needed
Problem: **Low-Power ≠ Power-Safe during Scan Capture**

<table>
<thead>
<tr>
<th>Circuit</th>
<th># of Gates</th>
<th># of FFs</th>
<th># of Clock Gators</th>
<th># of Test Vectors</th>
<th># of Risky Test Vec.</th>
<th>Ave. Sens. Paths / Vec.</th>
<th>Ave. Risky Paths / Vec.</th>
<th>CPU (sec.)</th>
<th># of Risky Vec. with Low WSA</th>
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<tr>
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<td>50K</td>
<td>1,077</td>
<td>66</td>
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<td>8</td>
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</tr>
<tr>
<td>Large</td>
<td>600K</td>
<td>35,566</td>
<td>984</td>
<td>191</td>
<td>11</td>
<td>0.2</td>
<td>3.8</td>
<td>2,772</td>
<td>5</td>
</tr>
</tbody>
</table>

**Local Capture Power Management Needed**
Next Stage
Paradigm Shift

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Coarse-Grained

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Power Reduction Only
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Now
Future

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Some Interesting R&D Topics (in random order)

- Power-Aware 3D Testing
- Power-Aware FPGA Testing
- Power-Aware On-Line Testing
- Low-Overhead Power-Safe BIST
- Right-Shift-Power Test Generation
- Power-Aware Fault Tolerance Design
- Right-Capture-Power Test Generation
- Fast and Accurate Power Safety Checking
- System-Level Power-Aware Test Scheduling
- Low-Overhead Power-Safe Scan Test Compression
- Fault Diagnosis and Silicon Debug of Low-Power Circuits
- IP with Power-Aware Test Infrastructure and Right-Power Test Data
- Seamless Power-Aware DFT based on CPF or UPF (IEEE Std. 1801-2009)
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An Example: Right-Capture-Power Test

No need to consider **dead areas**.

**Hot areas** must be removed by reducing local switching.

**Cold areas** may be made “warm” by increasing local switching.
High Functionality \rightarrow \text{Successful LSI Product} \rightarrow \text{Low Power}

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Test-Mode
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- Mail

- Growing Power Gap
- Higher Test Power (Needs to Handle PMS)

Test Crisis
- Excessive Heat • Timing Failures
- Higher Test Complexity due to PMS
- Damage / Low Yield / High Cost

Low Functional Power (Wide Use of PMS) \rightarrow \text{Low Power Design}

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THANK YOU

Let us make LSI test cool.