Power-Aware Testing for Low-Power VLSI Circuits

Xiaoqing Wen
Kyushu Institute of Technology
High Performance → Successful LSI Product → Low Power

Function-Mode
- Call
- Cam
- Web
- Mail

Test-Mode
- Call
- Cam
- Web
- Mail

Growing Power Gap

Low Functional Power (Wide Use of PMS)

High Test Power (Needs to Handle PMS)

Test Power Related Crisis
- Excessive Heat • Timing Failures
- Higher Test Complexity due to PMS

Test Power Related Crisis
- Damage / Low Yield / High Cost

Low Power Design

Power Aware Test
Outline

1. Test Power Problems
2. Power Analysis for Power-Aware Test
3. Power Management for Power-Aware Test
4. Future Research Topics
Outline

① Test Power Problems

② Power Analysis for Power-Aware Test

③ Power Management for Power-Aware Test

④ Future Research Topics
Impact of Test Power in At-Speed Scan Testing (LOC)

Shift Failure Capture Power (IR-Drop / L di/dt) – Induced Delay Increase and/or Clock Skew

Excessive Heat Shift Power Shift Failure

Accumulative Instantaneous Instantaneous Instantaneous Instantaneous

Many Shift Pulses Clock Skew in Clock Tree Capture Failure Delay Increase on Clock Path

Test Vector Load Started Test Vector Load Completed Launch Capture Response Capture

SE

CLK

C_1 C_2

Test Vector Load Started

Fast Test Cycle

Many Shift Pulses

Delay Increase on Long Sensitized Path

Excessive Delay Increase on Long Sensitized Path

Delay Increase on Clock Path

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Test Power Problems: \( P1 \sim P4 \)

- **P1**: Excessive Heat
  - Chip Damage
  - Reduced Reliability
  - High Test Cost

- **P2**: Shift Failure
- **P3**: Capture Failure
  - False-Test-Induced Yield Loss

- **P4**: Clock Stretch
  - Low Test Quality
  - Low Reliability
Power-Aware Test

- **Function-Test Power Gap**
- **Test Power Analysis**
- **Test Power Management**

Avoid Under-Kill

Avoid Over-Kill

**Functional Power**

**Test Power before**

**Test Power after**
Outline

1. Test Power Problems
2. Power Analysis for Power-Aware Test
3. Power Management for Power-Aware Test
4. Future Research Topics
Ideal vs. Reality

Switching Activity

- Accurate but costly.
- OK for sign-off but too expensive for use in DFT / ATPG.

- Fast and accurate-enough approximation needed.
- Layout / PDN aware gate-level metric preferred.

Temp. Analysis
IR-Drop Analysis + Delay Analysis
Sensitization Analysis

Excessive Heat
Excessive Delay along Sensitized / Clock Paths

Ideal
Reality

Ideal vs. Reality

- Accurate but costly.
- OK for sign-off but too expensive for use in DFT / ATPG.

- Fast and accurate-enough approximation needed.
- Layout / PDN aware gate-level metric preferred.
Power Estimation Metrics

- **P1**: Excessive Heat
- **P2**: Shift Failure
- **P3**: Capture Failure
- **P3**: Clock Stretch

**Excessive Heat for the Whole Circuit**

Whole-Circuit-Based Analysis

- **Global**

**Excessive Delay along Sensitized / Clock Paths**

Path-Based Analysis

- **Local**
Global Shift Power Analysis for Excessive Heat (P1)

Estimating Accumulative Impact of Shift Power

Weighted_Transitions = \sum (Scan\_Chain\_Length - Transition\_Position)

Switching in the CUT

Switching at FFs

Local Shift Power Analysis for Shift Failures (P2)

Estimating Inst. Impact of Shift Power on Clock

Timing failure

\[ \Delta WSA = |WSA_1 - WSA_2| \]

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Local Capture Power Analysis for Capture Failures (P3)

Estimating Impact of Capture Power on LSP

Impact Area of Path P

On-Path Gate G

Aggressor Region of Gate G

Long Sensitized Path P

WSA of the Impact Area of P

Large $\rightarrow$ $P$ is risky

Small $\rightarrow$ $P$ is safe

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Local Capture Power Analysis for Clock Stretch (P4)

Estimating Impact of Capture Power on Clock

Clock Stretch

excessive

SCK

FFi

WSA

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Outline

1️⃣ Test Power Problems
2️⃣ Power Analysis for Power-Aware Test
3️⃣ Power Management for Power-Aware Test
4️⃣ Future Research Topics
Requirements of Power-Aware Test

- Temperature-Safety
- Shift-Failure-Safety
- Capture-Failure-Safety
- Clock-Stretch-Safety
Capture-Failure-Safety

Rescue & Mask
For Capture-Failure-Safety: Example

- **Conventional**
  - Detection-Oriented Test Cube Generation
  - Detection-Oriented X-Filling (Random-Fill, etc.)

- **Rescue**
  - X-Restoration for Risky Paths
  - X-Filling for Reducing Capture WSA

- **Mask**
  - Remaining Risky Path Masking

Path Classification

- Impact X-Bits

For Capture-Failure-Safety: Results (Commercial ATPG)

<table>
<thead>
<tr>
<th>Circuit</th>
<th># of Vectors</th>
<th>% Risky Vectors</th>
<th>FC (%)</th>
<th>BCE (%)</th>
<th>SDQL</th>
<th>CPU (Sec.)</th>
</tr>
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<tbody>
<tr>
<td>b17</td>
<td>1,568</td>
<td>3.8</td>
<td>82.8</td>
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<td>491</td>
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<td>2,592</td>
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<td>46.6</td>
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<td>43.1</td>
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<td>264</td>
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<td>b21</td>
<td>1,330</td>
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<td>83.1</td>
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<td>b22</td>
<td>1,444</td>
<td>13.0</td>
<td>81.4</td>
<td>44.2</td>
<td>255.7</td>
<td>533</td>
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</table>

- Risky test vectors (i.e., vectors with risky paths) do exist.
- Metrics for assessing test quality:
  - **FC**: Fault Coverage
  - **BCE**: Bridge Coverage Estimate
  - **SDQL**: Small Delay Quality Level
For **Capture-Failure-Safety**: Results (Proposed ATPG)

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Δ# of Vectors (%)</th>
<th>% Risky Vectors</th>
<th>ΔFC (%)</th>
<th>ΔBCE (%)</th>
<th>ΔSDQL (%)</th>
<th>CPU (Sec.)</th>
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</thead>
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<td>b17</td>
<td>0.20</td>
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<td>-2.02</td>
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<td>-0.07</td>
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<td>+0.63</td>
<td>532</td>
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<td>b21</td>
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<td>0</td>
<td>0.05</td>
<td>-1.10</td>
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<td>b22</td>
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<td>0</td>
<td>0.11</td>
<td>-0.68</td>
<td>-2.03</td>
<td>1,150</td>
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</table>

- **Capture-failure-safety is guaranteed.**
- **Impact on and test data volume is insignificant.**
- **Impact on test quality (FC, BCE, SDQL) is negligible.**
ATPG for Capture-Failure-Safety & Clock-Stretch-Safety

Capture-Failure-Safety

Clock-Stretch-Safety

Rescue & Mask & Reduction
### ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

#### Example (1/2)

<table>
<thead>
<tr>
<th>Conventional</th>
<th>Detection-Oriented X-Filling (Random-Fill, etc.)</th>
<th>X-Restoration for Risky Paths</th>
<th>P-II (Risky Path Elimination)</th>
<th>Remaining Risky Path Masking</th>
<th>Non-Impact Change Bit Release</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Cube Generation w/ Dynamic Compaction</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>C</td>
<td>C</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>a 0</td>
<td>a 0</td>
<td>a 0</td>
<td>a 0</td>
<td>a 0</td>
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<td>b X</td>
<td>b 1</td>
<td>b 0</td>
<td>b 0</td>
<td>b 0</td>
<td>b 0</td>
</tr>
<tr>
<td>c X</td>
<td>c 0</td>
<td>c 0</td>
<td>c 0</td>
<td>c 0</td>
<td>c 0</td>
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<tr>
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<td>d 1</td>
<td>d 1</td>
<td>d 1</td>
<td>d 1</td>
</tr>
<tr>
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</tr>
<tr>
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<tr>
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<td>g 1</td>
<td>g 1</td>
<td>g 1</td>
<td>g 1</td>
<td>g 1</td>
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<tr>
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<td>h 1</td>
<td>h 1</td>
<td>h 1</td>
<td>h 1</td>
<td>h 1</td>
</tr>
<tr>
<td>i X</td>
<td>i 1</td>
<td>i 1</td>
<td>i 1</td>
<td>i 1</td>
<td>i 1</td>
</tr>
</tbody>
</table>

#### P-I (Risky Path Checking)
ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

Example (2/2)
## ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

### Results (Commercial ATPG)

<table>
<thead>
<tr>
<th>Circuit</th>
<th># of Gates</th>
<th># of FFs</th>
<th>Max. Path Length</th>
<th># of Vectors</th>
<th>FC (%)</th>
<th>BCE (%)</th>
<th>SDQL</th>
<th># Risky Paths</th>
<th>Ave. WSAcp</th>
<th>CPU (Sec.)</th>
<th>Δ# of Vectors (%)</th>
<th># Risky Paths</th>
</tr>
</thead>
<tbody>
<tr>
<td>b17</td>
<td>32326</td>
<td>1415</td>
<td>34</td>
<td>1175</td>
<td>70.1</td>
<td>67.2</td>
<td>16.3</td>
<td>31</td>
<td>167</td>
<td>674</td>
<td>141.2</td>
<td>68</td>
</tr>
<tr>
<td>b18</td>
<td>114621</td>
<td>3320</td>
<td>47</td>
<td>2428</td>
<td>63.6</td>
<td>64.8</td>
<td>198.9</td>
<td>172</td>
<td>400</td>
<td>5901</td>
<td>116.2</td>
<td>572</td>
</tr>
<tr>
<td>b19</td>
<td>231320</td>
<td>6642</td>
<td>68</td>
<td>3327</td>
<td>64.6</td>
<td>64.9</td>
<td>290.0</td>
<td>230</td>
<td>425</td>
<td>8175</td>
<td>182.3</td>
<td>809</td>
</tr>
<tr>
<td>b20</td>
<td>20226</td>
<td>490</td>
<td>45</td>
<td>1896</td>
<td>92.9</td>
<td>59.2</td>
<td>115.1</td>
<td>0</td>
<td>420</td>
<td>169</td>
<td>59.4</td>
<td>2</td>
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<tr>
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<td>20571</td>
<td>490</td>
<td>44</td>
<td>1870</td>
<td>93.2</td>
<td>58.9</td>
<td>134.7</td>
<td>0</td>
<td>573</td>
<td>139</td>
<td>55.5</td>
<td>4</td>
</tr>
<tr>
<td>b22</td>
<td>29951</td>
<td>735</td>
<td>50</td>
<td>2303</td>
<td>93.7</td>
<td>63.8</td>
<td>139.4</td>
<td>83</td>
<td>644</td>
<td>483</td>
<td>39.3</td>
<td>120</td>
</tr>
</tbody>
</table>

- Test data inflation is large.
- Risks of capture failures remain even with LCP-ATPG vectors.
ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

Results (Proposed ATPG)

- Test data inflation is very small.
- Impact on test quality (FC, BCE, SDQL) is negligible.
- Capture-failure-safety is guaranteed.
- Clock stretch is significantly reduced.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>P-II</th>
<th>P-III</th>
<th>Proposed ATPG</th>
</tr>
</thead>
<tbody>
<tr>
<td>b17</td>
<td>32.3</td>
<td>45.6</td>
<td>4.7 0.1 0.1 -0.9 38 0 -8.4 982</td>
</tr>
<tr>
<td>b18</td>
<td>17.9</td>
<td>53.7</td>
<td>4.2 0.0 0.5 -0.1 335 0 -23.8 7078</td>
</tr>
<tr>
<td>b19</td>
<td>32.2</td>
<td>22.5</td>
<td>3.6 0.0 0.3 0.3 149 0 -14.8 14079</td>
</tr>
<tr>
<td>b20</td>
<td>N/A</td>
<td>39.5</td>
<td>8.3 0.0 1.2 -0.1 0 0 -15.0 271</td>
</tr>
<tr>
<td>b21</td>
<td>N/A</td>
<td>35.8</td>
<td>4.9 0.0 1.2 -0.5 0 0 -0.9 149</td>
</tr>
<tr>
<td>b22</td>
<td>16.1</td>
<td>36.1</td>
<td>12.6 0.0 1.2 -1.0 210 0 -18.5 379</td>
</tr>
<tr>
<td>Ave.</td>
<td>24.6</td>
<td>38.8</td>
<td>6.4 0.0 0.8 -0.4 122 0 -13.6</td>
</tr>
</tbody>
</table>

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Outline

1. Test Power Problems
2. Power Analysis for Power-Aware Test
3. Power Management for Power-Aware Test
4. Future Research Topics
Topic #1: GPU-Based Electrical-Level Test Power Analysis

- Which test vector is test-power-risky?
- What is the problem (P1~P4)?
- Where is the problem?

Full-Timing Electrical-Level Test Power Analysis Needed
Topic #2: Advanced Test Power Management

Test Power Problems

P1 Excessive Heat
P2 Shift Failure
P3 Capture Failure
P4 Clock Stretch
Topic #3: Right-Power Test

- **Low-Power Test**
  - reduce only

- **Power-Safe Test**
  - reduce + mask

- **Right-Power Test**
  - reduce + mask + increase
No need to consider **dead areas**.

**Hot areas** must be removed by reducing local switching.

**Cold areas** may be made “**warm**” by increasing local switching.
High Performance → Successful LSI Product → Low Power

Function-Mode
Call
Cam
Web
Mail
Low Functional Power
(Wide Use of PMS)

Test-Mode
Call
Cam
Web
Mail
High Test Power
(Needs to Handle PMS)

Growing Power Gap

Test Crisis
Excessive Heat • Timing Failures
Higher Test Complexity due to PMS
(Damage / Low Yield / High Cost)

Low Power Design
Power Aware Test

Test
Function
LSI

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THANK YOU

Let us make LSI test *cool.*