2015 Joint Workshop on Dependable Integrated Systems
September 3, 2015
Conference Room E, Denki Building, 2-1-82, Watanabe Ave., Chuo-Ku, Fukuoka, Japan

■ 13:20~13:30 Opening
  S. Kajihara, Kyushu Institute of Technology, Japan
  H.-J. Wunderlich, University of Stuttgart, Germany

■ 13:30~14:00 Presentation 1
  • Intermittent and Transient Fault Diagnosis on Sparse Code Signatures
    M. A. Kochte, University of Stuttgart, Germany

■ 14:00~14:30 Presentation 2
  • Power Related Analysis for LSI and Motion Analysis for Baseball
    K. Miyase, Kyushu Institute of Technology, Japan

■ 14:30~15:00 Break

■ 15:00~15:30 Presentation 3
  • GPU-Accelerated Small Delay Fault Simulation
    E. Schneider, University of Stuttgart, Germany

■ 15:30~16:00 Presentation 4
  • Logic/Clock-Path-Aware At-Speed Scan Test Generation and Fault Simulation
    S. Holst, Kyushu Institute of Technology, Japan

■ 16:00~17:00 Project Review and Planning
  Kyushu Institute of Technology, Japan
  University of Stuttgart, Germany

■ 17:00~17:05 Closing
  X. Wen, Kyushu Institute of Technology, Japan

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