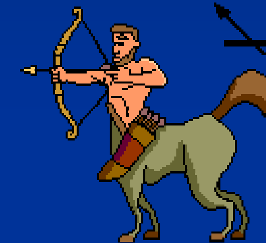
Low-Power Testing

for Low-Power Devices

Test

Power



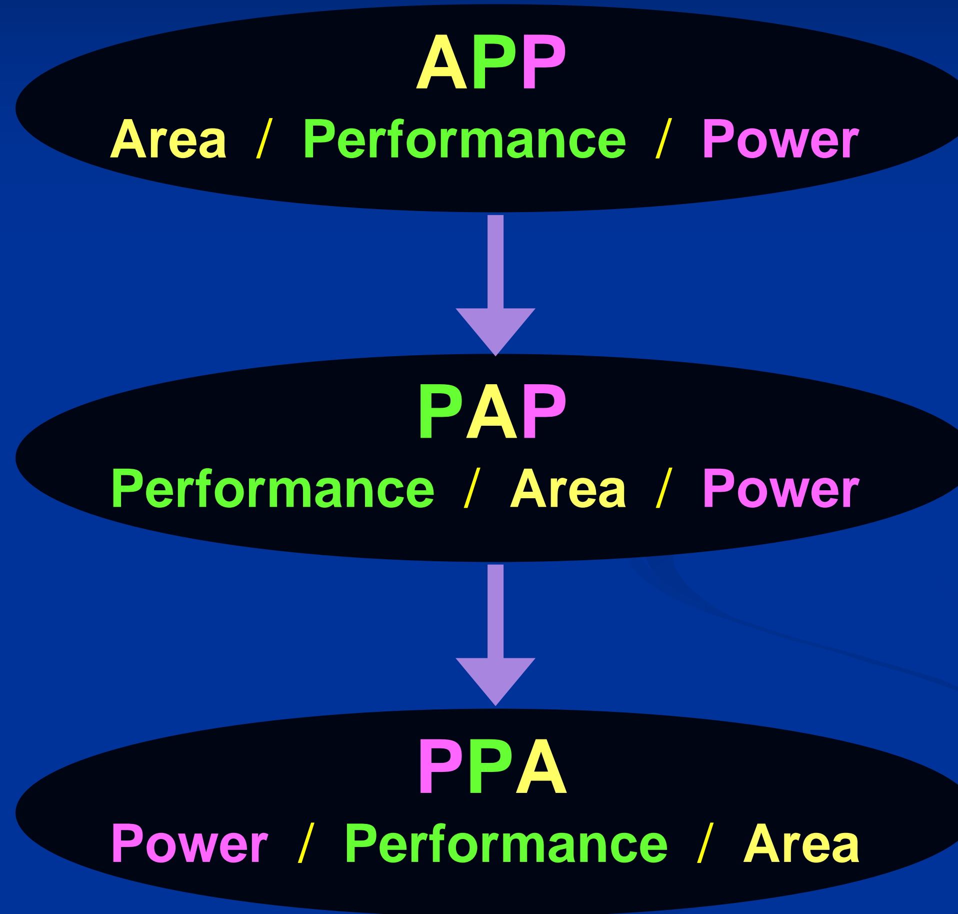
Xiaoqing Wen

Kyushu Institute of Technology

wen@cse.kyutech.ac.jp

Critical Elements in IC Industry

*Area * Performance * Power*

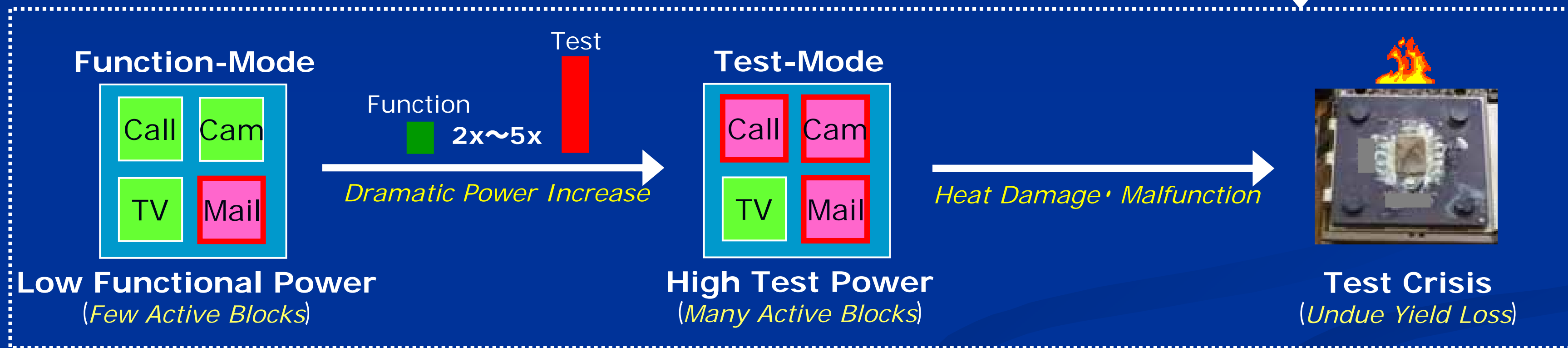


(Inspired by A. Bose, ATS Keynote Speech, 2010)

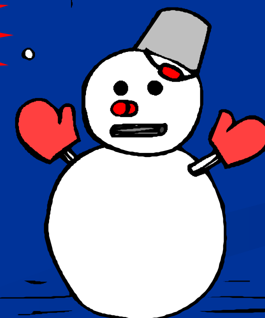
© X. WEN 2010. All Rights Reserved.

Basic Message

High Functionality → Success in IC Industry ← Low Power



Low-Power Design



Low-Power Test

A Cool Product

© X. WEN 2010. All Rights Reserved.

Outline

1. Risk of Low-Power LSI Circuits in Testing
2. Basic Strategy to Test Power Reduction
3. Shift Power Reduction
4. Capture Power Reduction
5. New Research Opportunities
6. Summary

© X. WEN 2010. All Rights Reserved.

Outline

1. Risk of Low-Power LSI Circuits in Testing
2. Basic Strategy to Test Power Reduction
3. Shift Power Reduction
4. Capture Power Reduction
5. New Research Opportunities
6. Summary

© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing

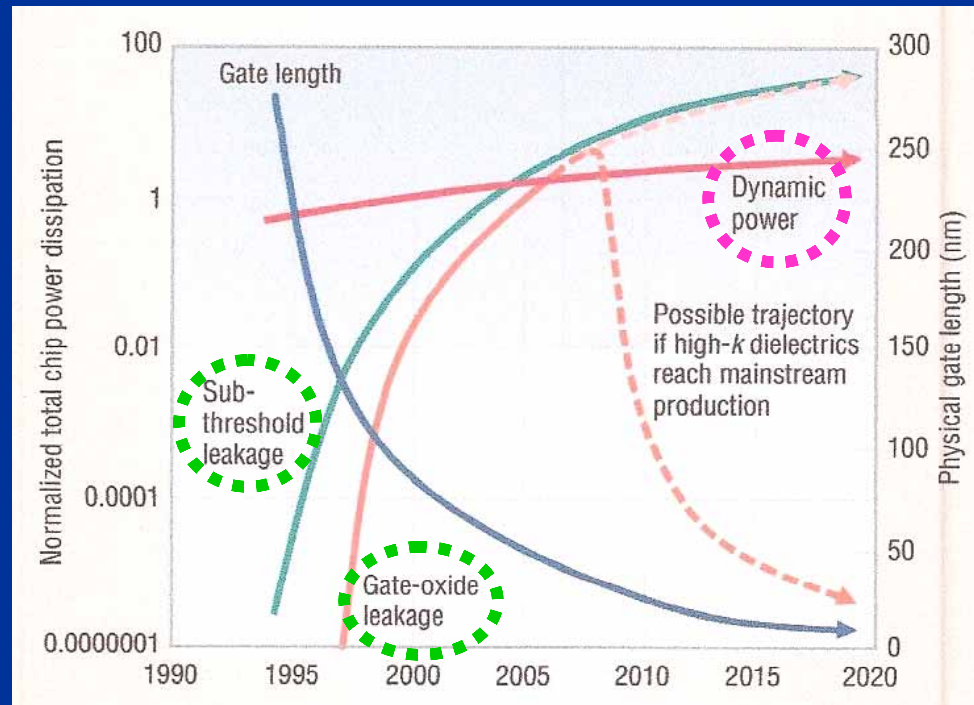
CMOS Power and Its Trend

Static Power

$P_{subthrehold_leakage}$
$P_{gate\text{-}oxide_leakage}$

Dynamic Power

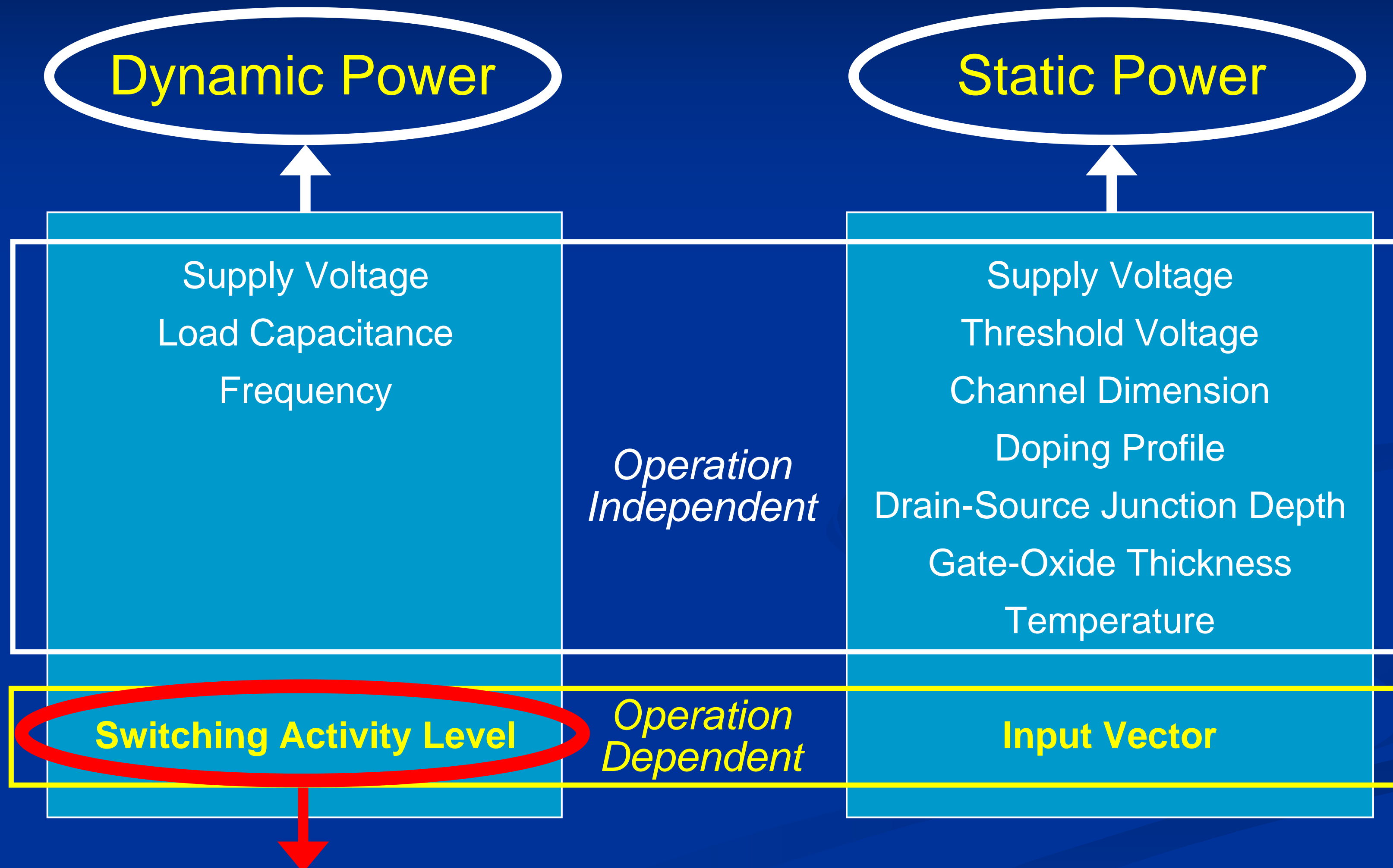
$P_{charge/discharge}$
$P_{short\text{-}circuit}$



(N. S. Kim et al., *IEEE Computer*, pp. 68-75, 2003)

© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing



Different for Function-Mode and Test-Mode.

© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing

Example of Low-Power Design

External Power Supply

ON / OFF
VDD1
VDD1
VDD2

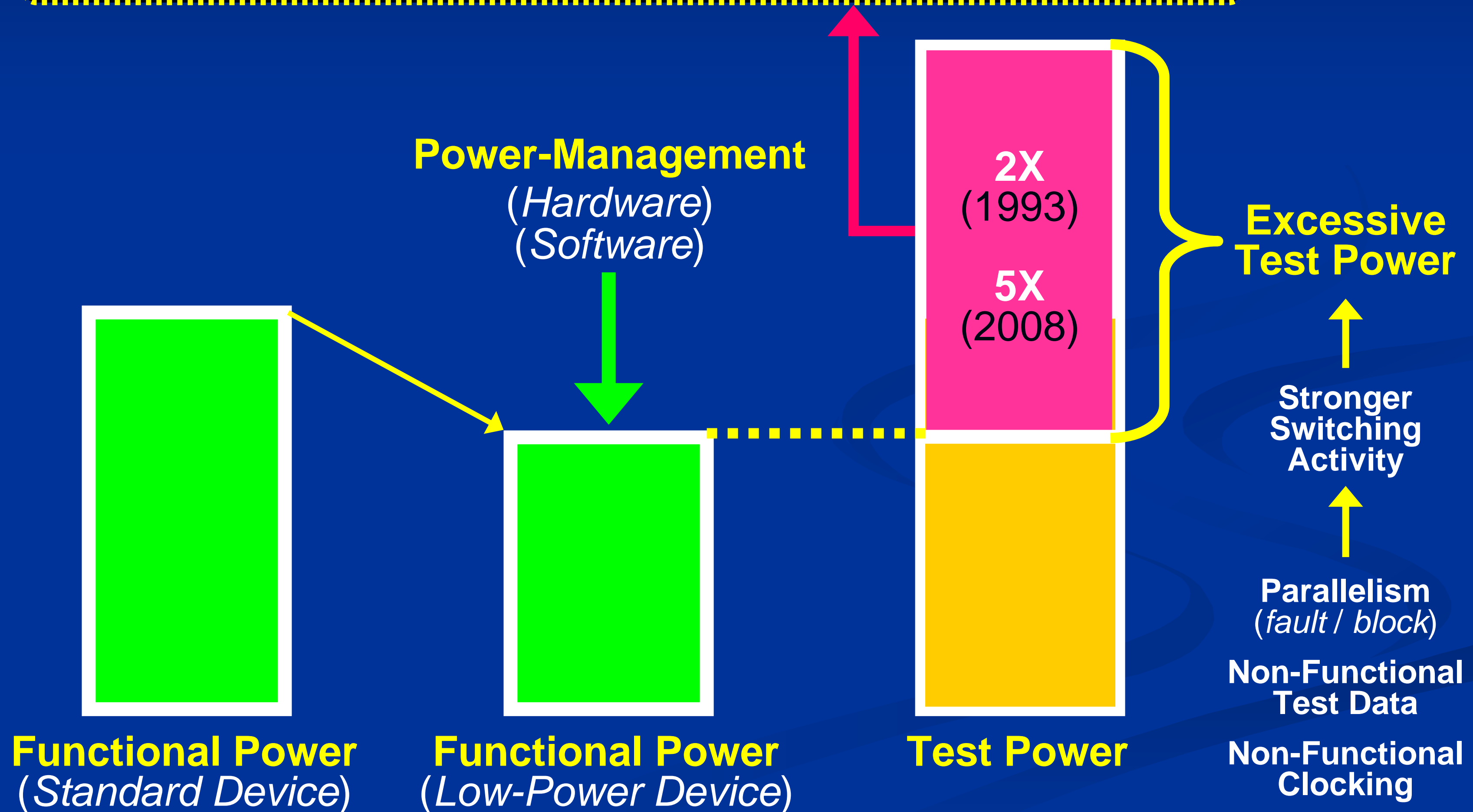
Power Controller
iso_enable
ack
req
Power Switch
stop_clock / save / restore
ack
Power Domain 1
(Conditionally ON)
RR
Isolation Cell
Enabled Level Shifter
Power Domain 2
(Always ON)
<Clock-Gating>
Level Shifter
Power Domain 3
(Always ON)
<Clock-Gating>
PD_TOP
(Always ON)

Extremely Low Functional Power Achieved

© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing

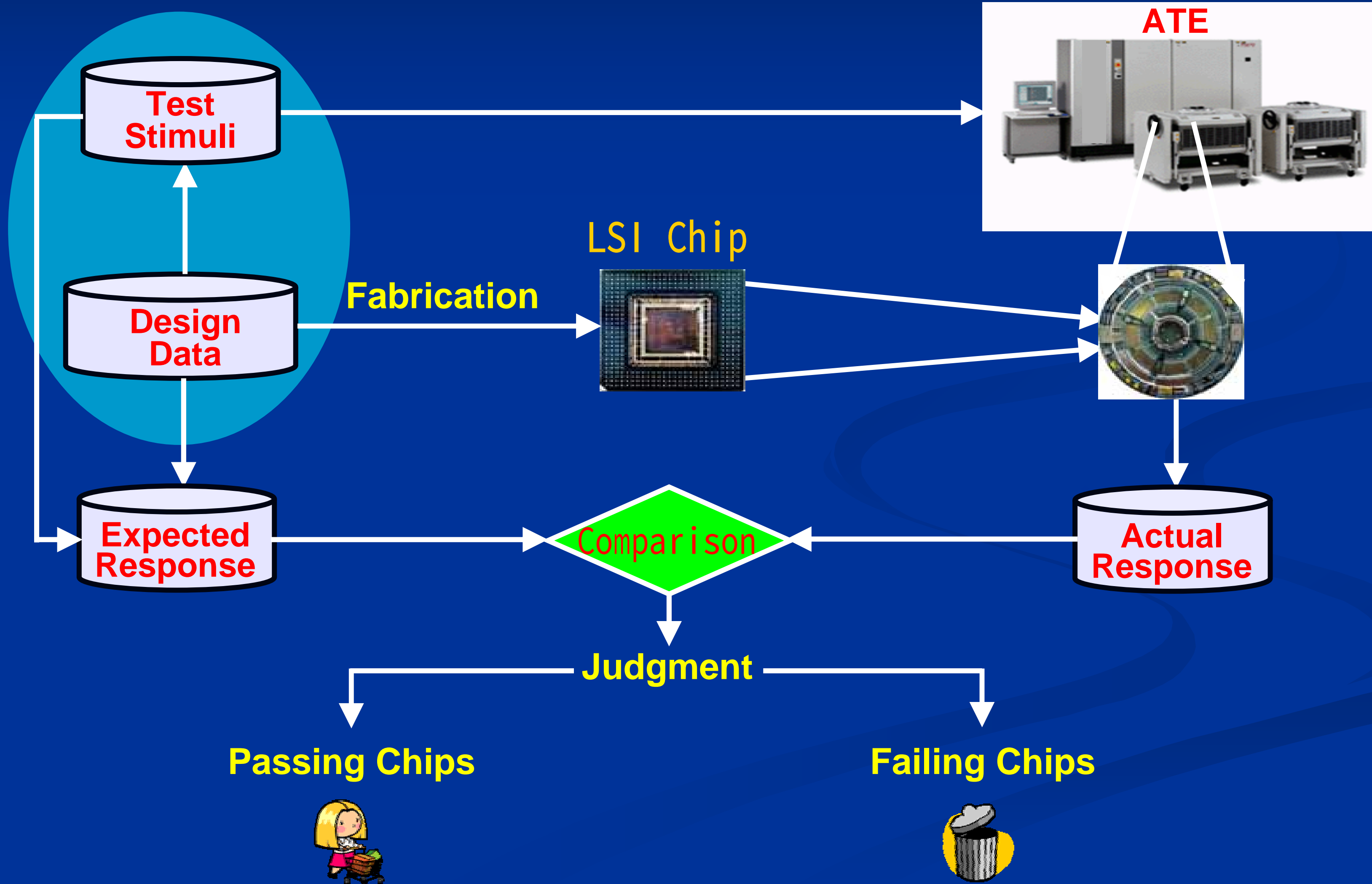
Low Functional Power ≠ Low Test Power



© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing

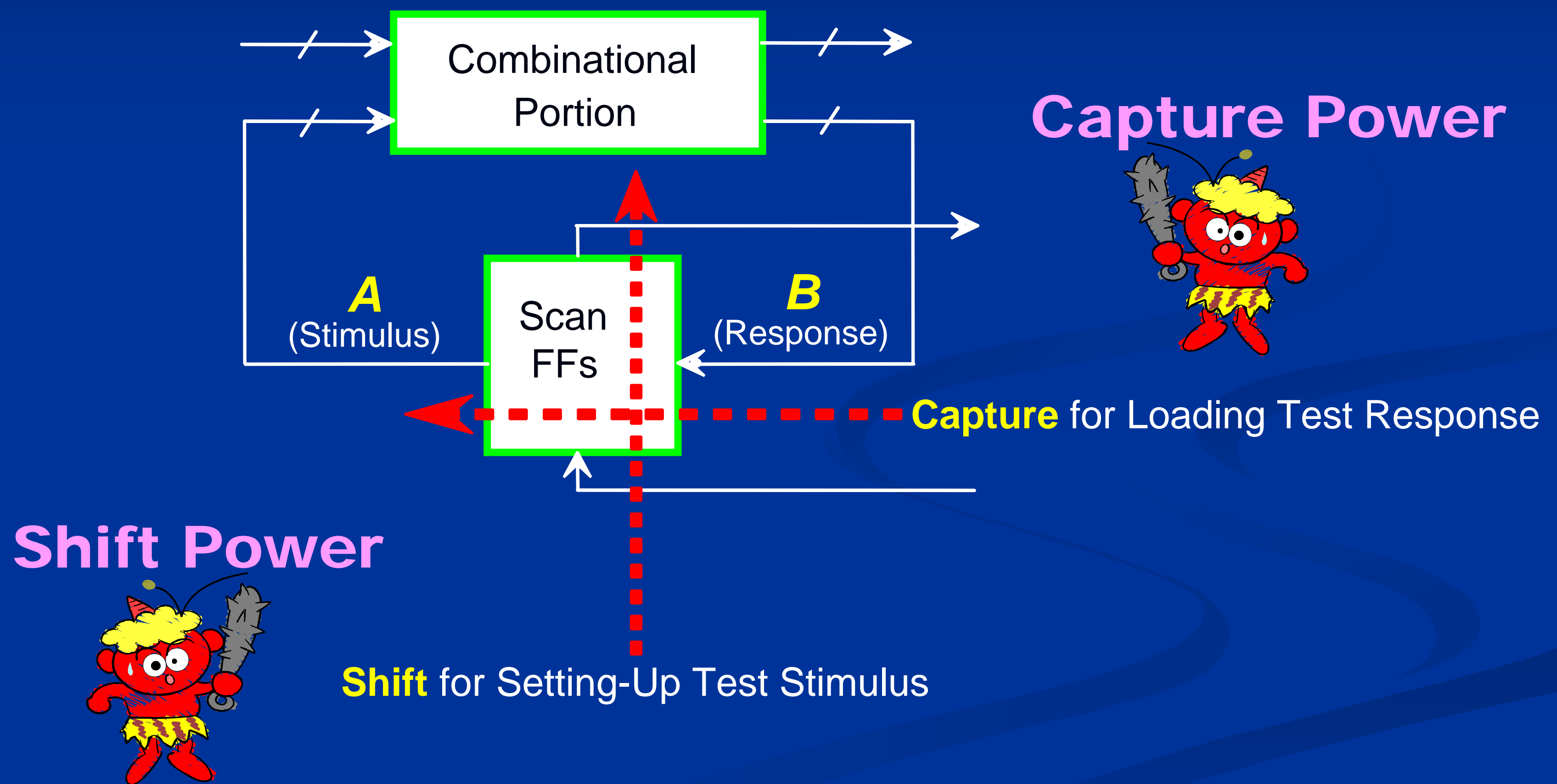
General Flow of LSI Testing



© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing

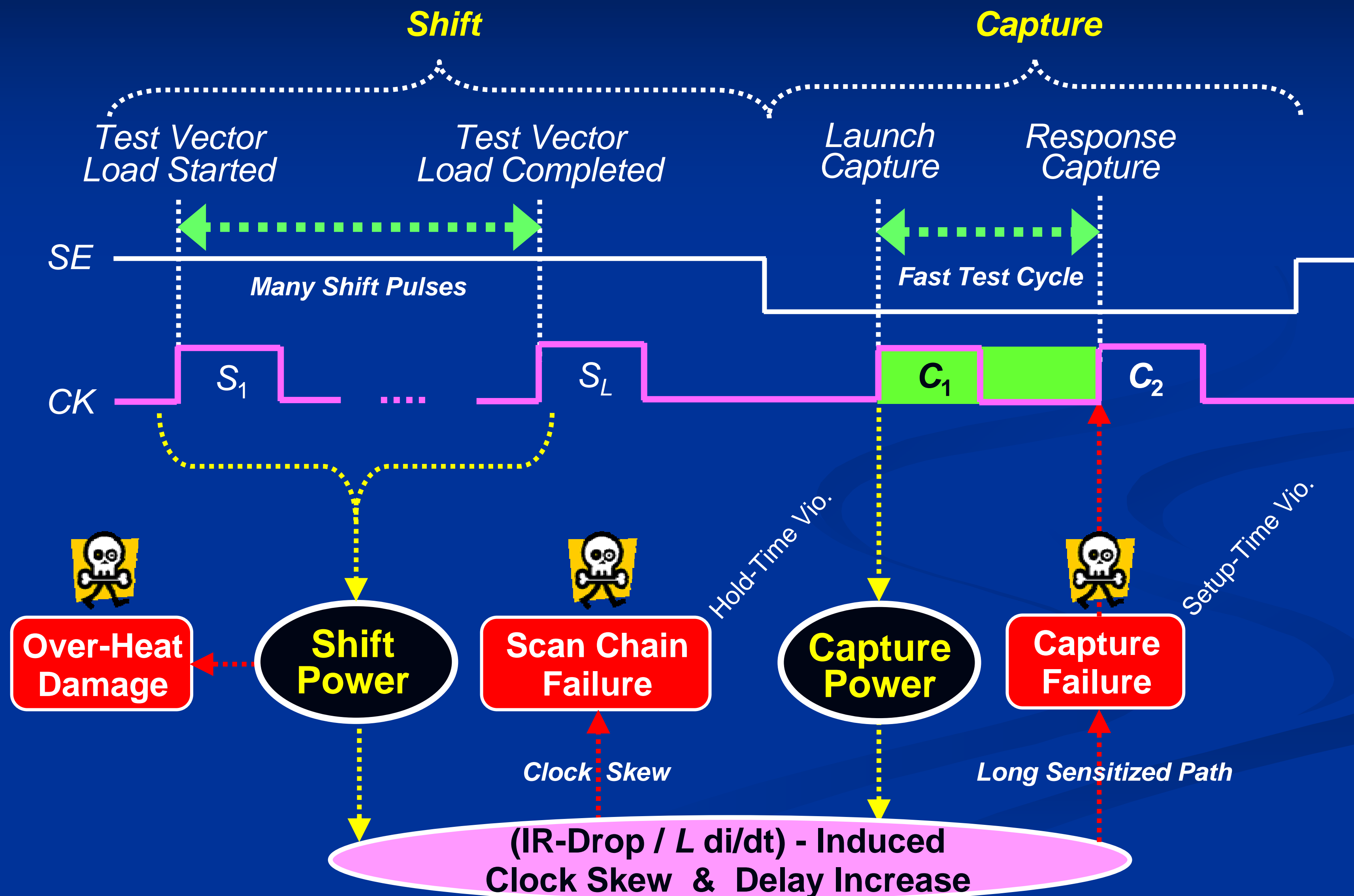
Shift Power and Capture Power



© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing

Impact of Test Power in At-Speed Scan-Based LSI Testing



© X. WEN 2010. All Rights Reserved.

1. Risk of Low-Power LSI Circuits in Testing

Consequences

Good chips may be *damaged* or may *fail* in LSI testing.

Undue (*No-Defect*) Yield Loss

Big Financial Loss

New High-Performance MPU

A Few Hundreds US$

Low-power design cannot be realized without low-power test !

© X. WEN 2010. All Rights Reserved.

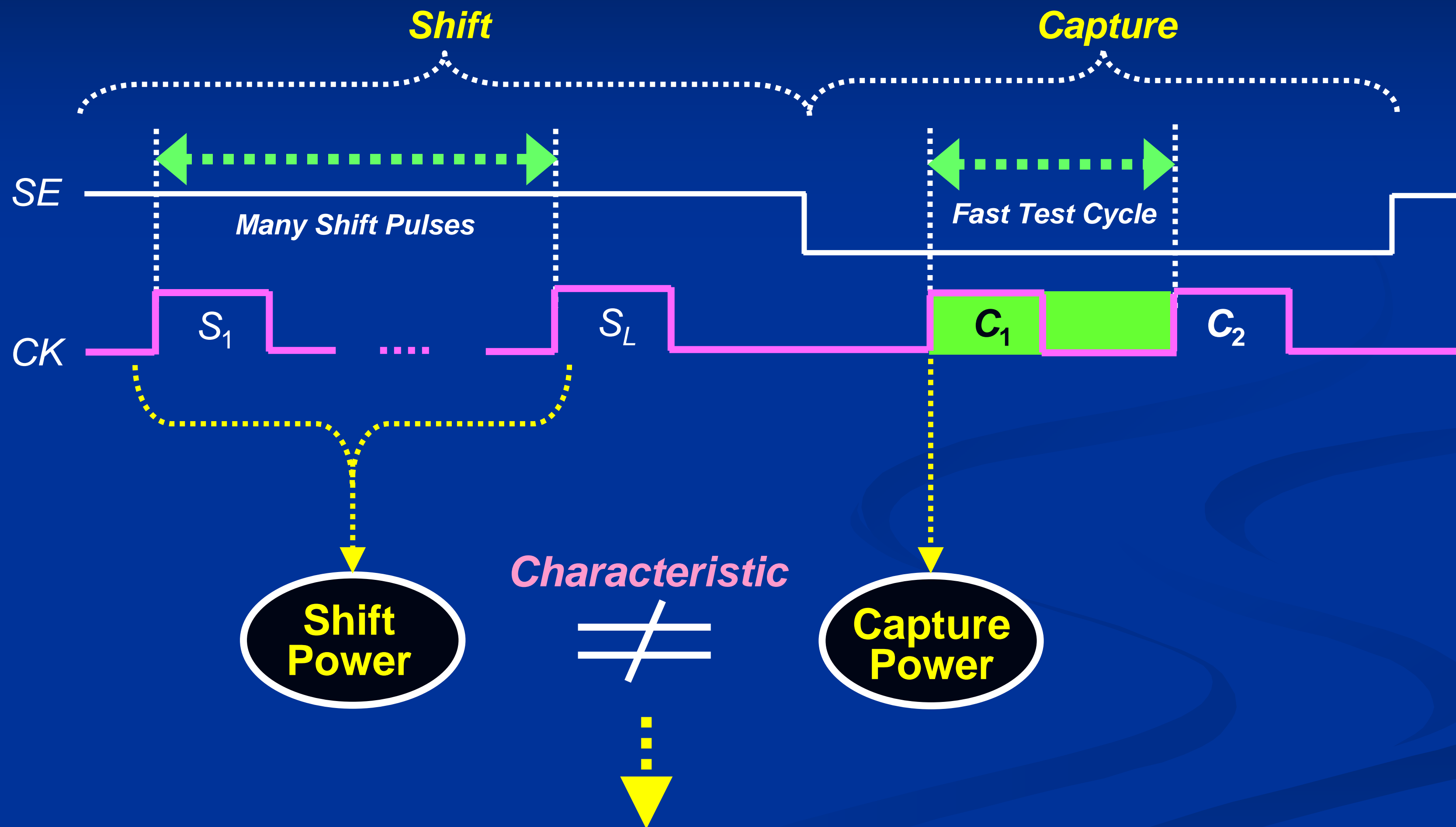
Outline

1. Risk of Low-Power LSI Circuits in Testing
2. **Basic Strategy to Test Power Reduction**
3. Shift Power Reduction
4. Capture Power Reduction
5. New Research Opportunities
6. Summary

© X. WEN 2010. All Rights Reserved.

2. Basic Strategy to Test Power Reduction

Shift Power and Capture Power

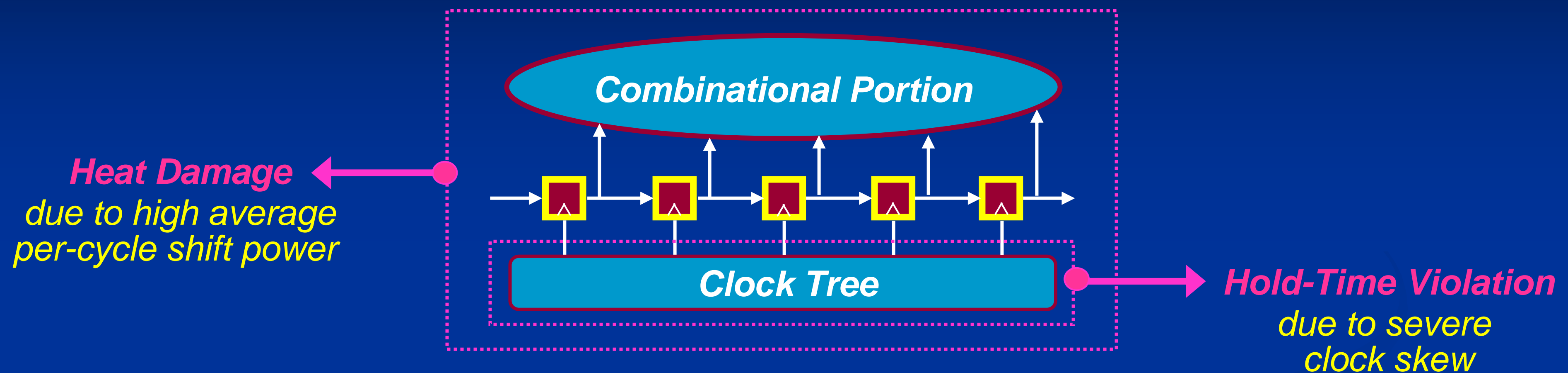


Different Reduction Strategies Needed

© X. WEN 2010. All Rights Reserved.

2. Basic Strategy to Test Power Reduction

Characteristics of Shift Power

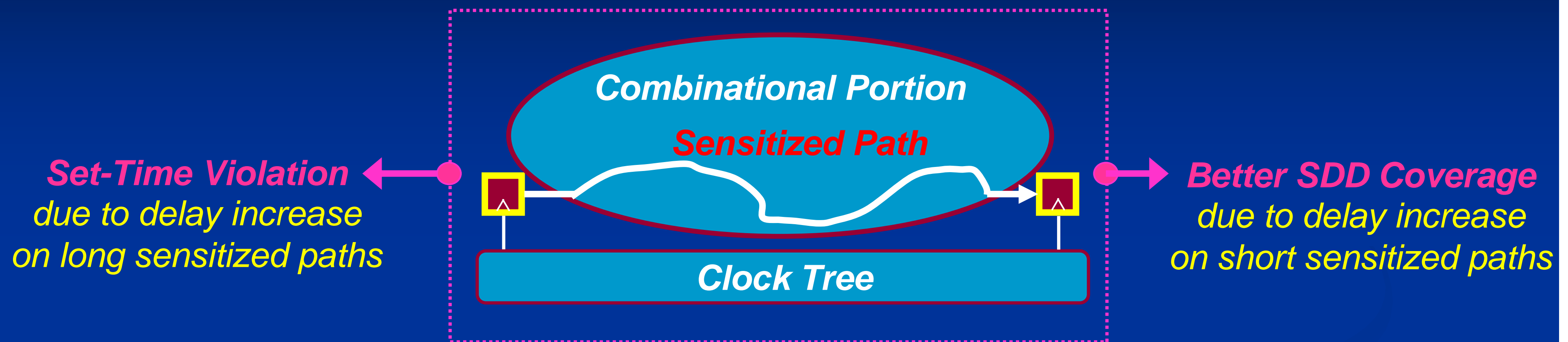


- ➔ *Shifting a pattern, even a functional one, may cause heavy switching.*
- ➔ *IR-drop may be worse in shift mode than in capture mode.*
- ➔ *All test vectors may have the shift power problem.*
- ➔ *Slow shift frequencies help reduce heat impact but not clock skew.*
- ➔ *Circuit / clock change has no impact on ATPG, time, size, and coverage.*
- ➔ *Only scan chains need to be considered as sensitized paths.*

© X. WEN 2010. All Rights Reserved.

2. Basic Strategy to Test Power Reduction

Characteristics of Capture Power

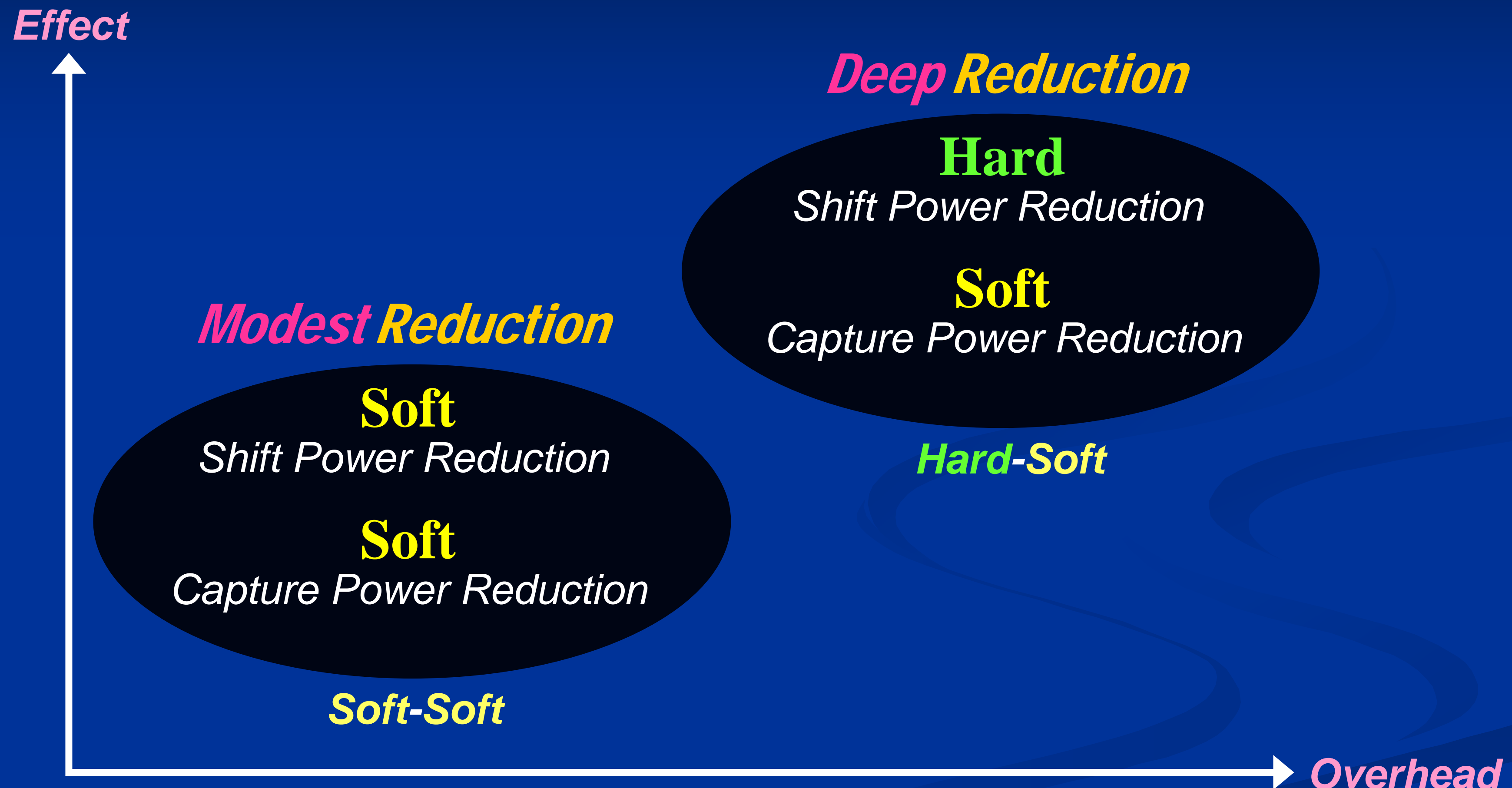


- ➔ *The impact of capture power depends on sensitized paths.*
- ➔ *Reducing capture power may be needed to avoid yield loss.*
- ➔ *Increasing capture power may help to improve test quality.*
- ➔ *Circuit / clock change may impact ATPG, time, size, and coverage.*
- ➔ *Capture power is highly dependent on the content of a pattern.*
- ➔ *Power management circuitry can be used for capture power reduction.*
- ➔ *A small number of test vectors suffers from the capture power problem.*

© X. WEN 2010. All Rights Reserved.

2. Basic Strategy to Test Power Reduction

Integrated Reduction of Both Shift and Capture Power



Type of Solution
- **Soft:** Test Data Manipulation
- **Hard:** Circuit Modification

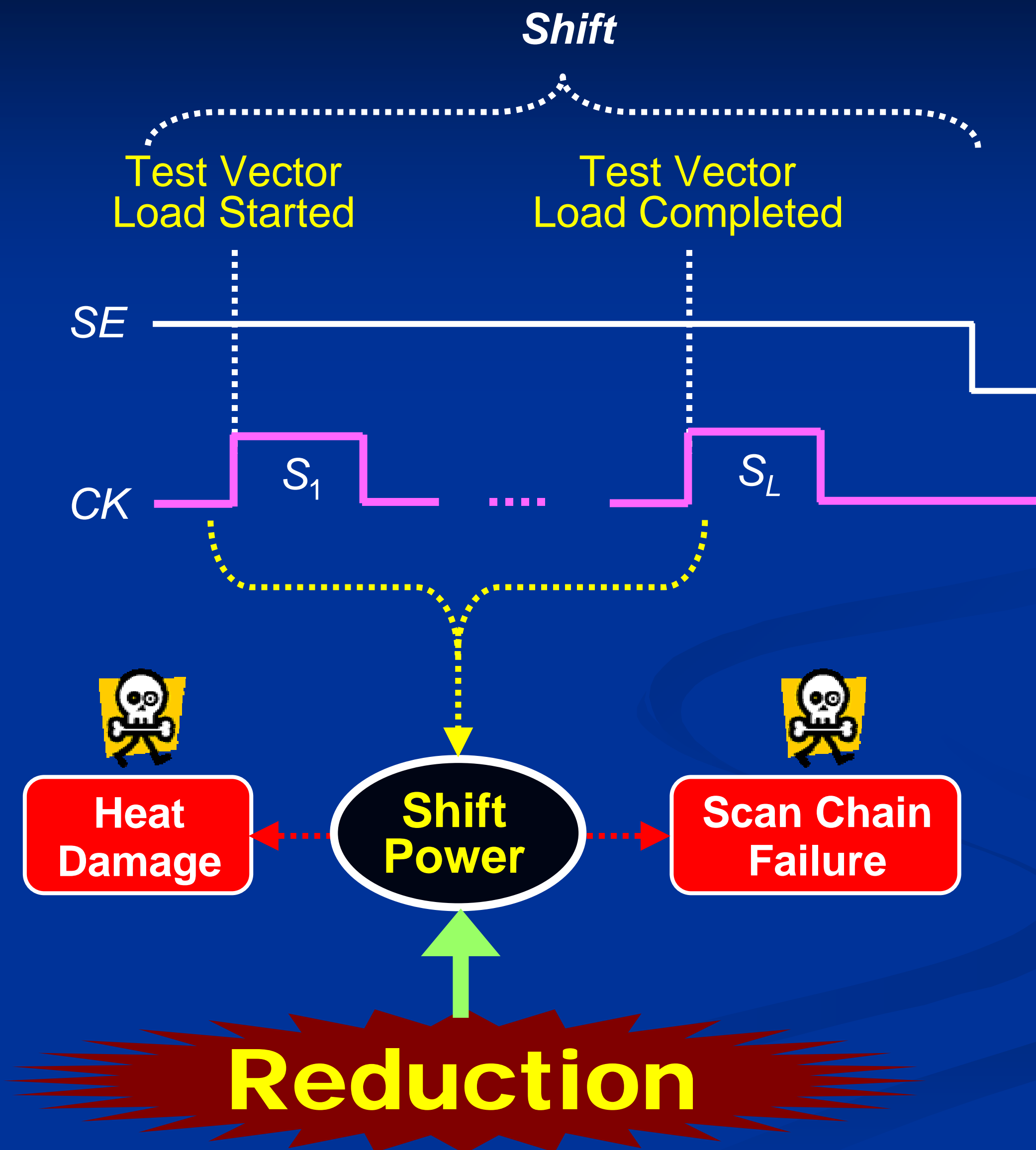
© X. WEN 2010. All Rights Reserved.

Outline

1. Risk of Low-Power LSI Circuits in Testing
2. Basic Strategy to Test Power Reduction
3. **Shift Power Reduction**
4. Capture Power Reduction
5. New Research Opportunities
6. Summary

© X. WEN 2010. All Rights Reserved.

3. Shift Power Reduction

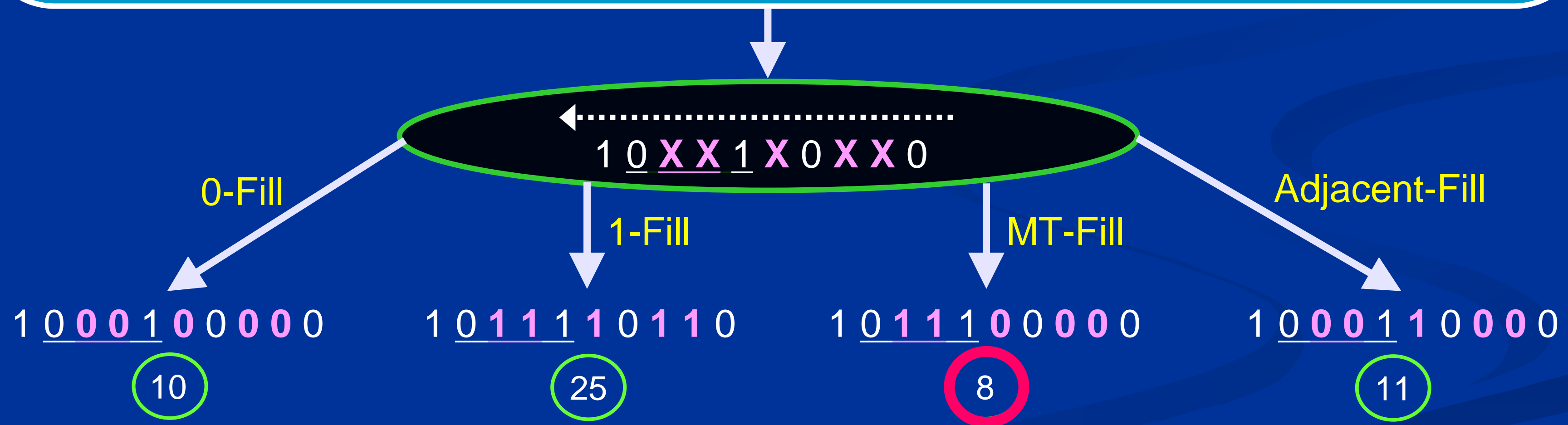


© X. WEN 2010. All Rights Reserved.

3. Shift Power Reduction (SOFT)

Low-Shift-Power X-Filling

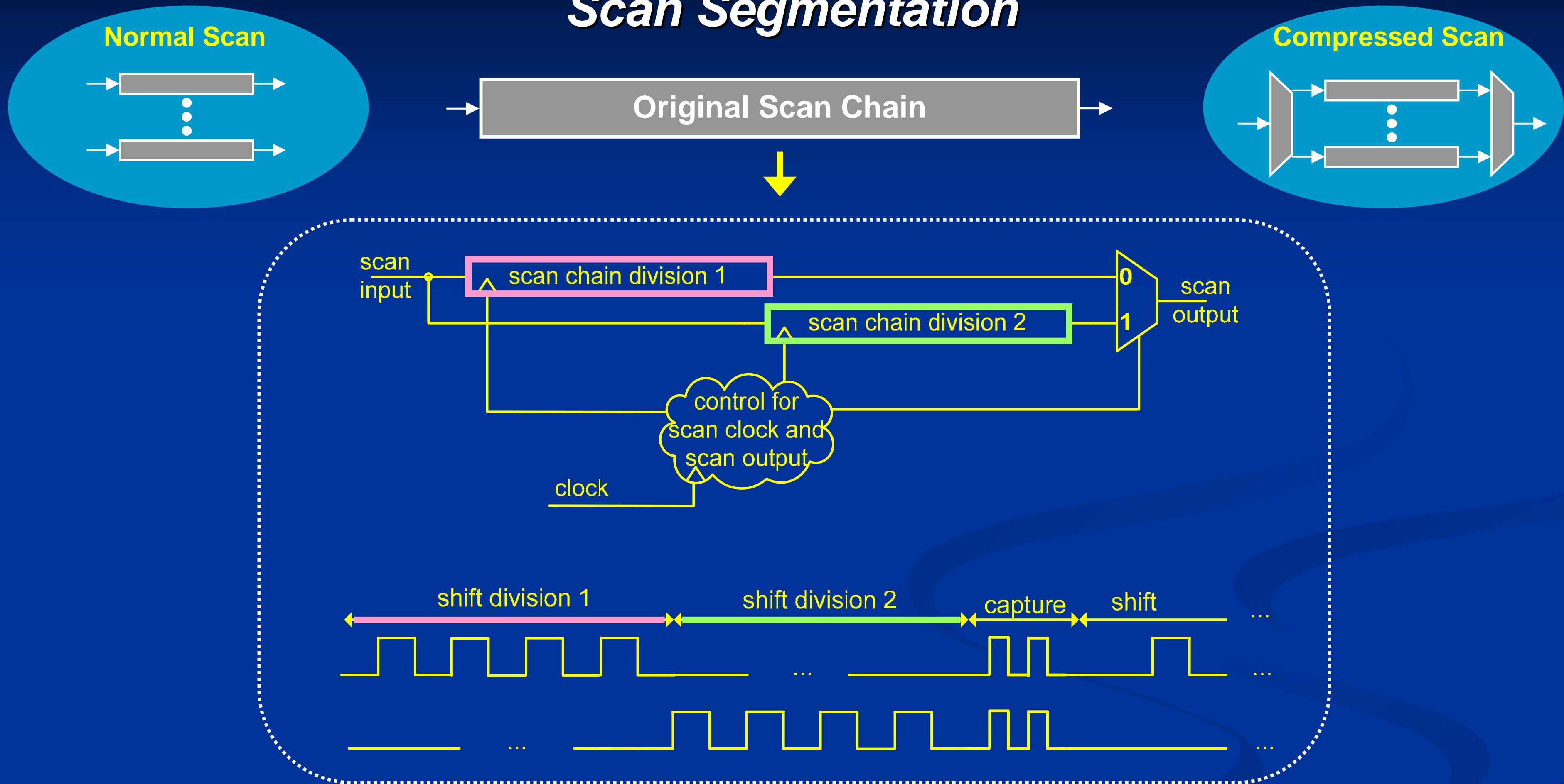
- 0-Fill → Fill all *X*-strings with 0.
- 1-Fill → Fill all *X*-strings with 1.
- MT-Fill → If the specified bits on both sides of an *X*-string have the same logic value, the *X*-string is filled with that logic value; if the specified bits on the two sides of an *X*-string have opposite logic values, the *X*-string is filled with an arbitrary logic value.
- Adjacent-Fill → Fill an *X*-string with the nearest specified-bit in the shift direction.



Easy to implement. / No circuit overhead.
Limited effect in test compression environments. / Test data increase.

© X. WEN 2010. All Rights Reserved.

3. Shift Power Reduction (Hard)



Predictable and data-independent shift (in & out) power reduction.
No change to ATPG and no increase in test application time.

© X. WEN 2010. All Rights Reserved.

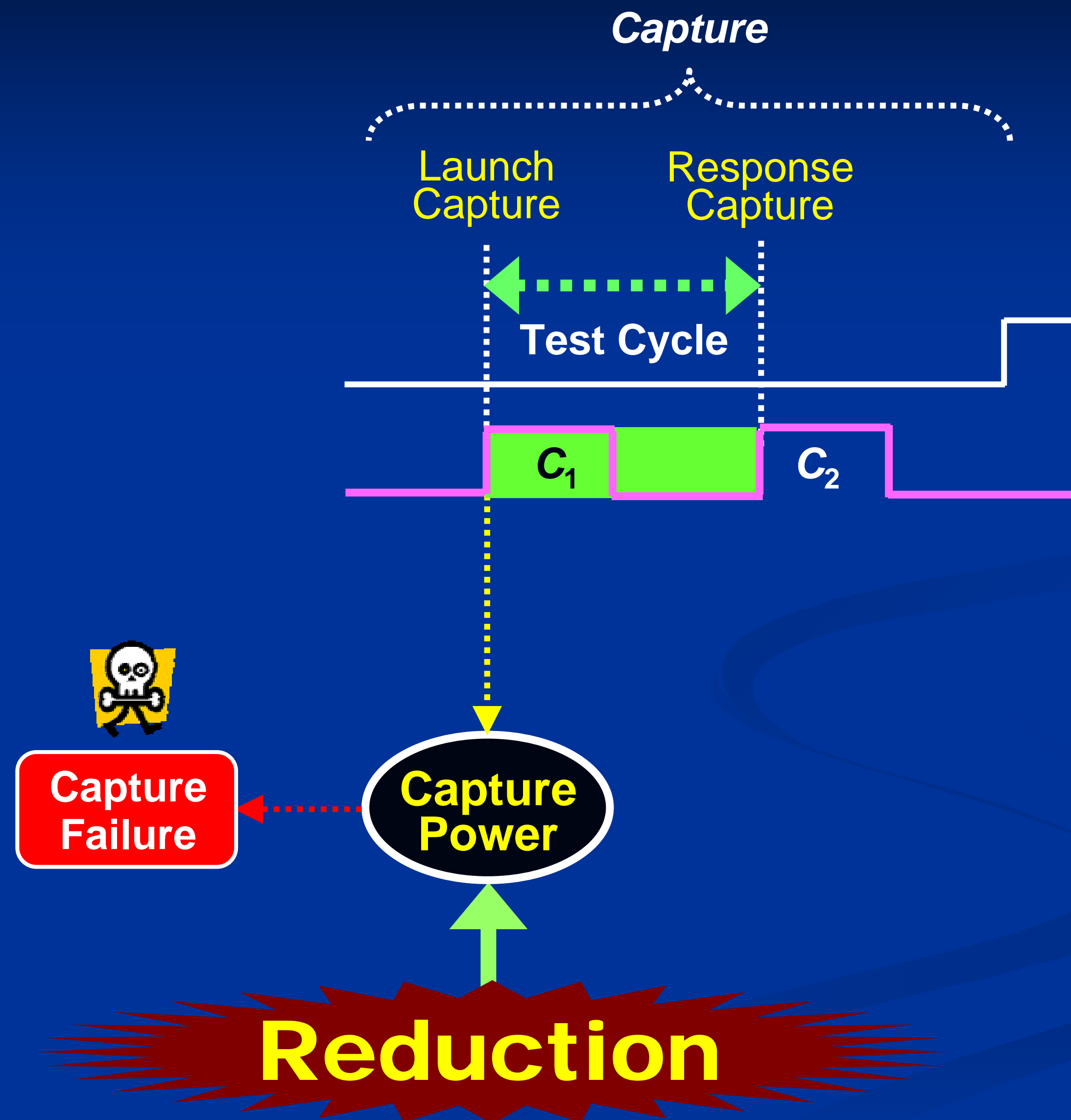
(L. Whetsel. al., *Proc. ITC*, pp. 863-872, 2000)

Outline

1. Risk of Low-Power LSI Circuits in Testing
2. Basic Strategy to Test Power Reduction
3. Shift Power Reduction
4. **Capture Power Reduction**
5. New Research Opportunities
6. Summary

© X. WEN 2010. All Rights Reserved.

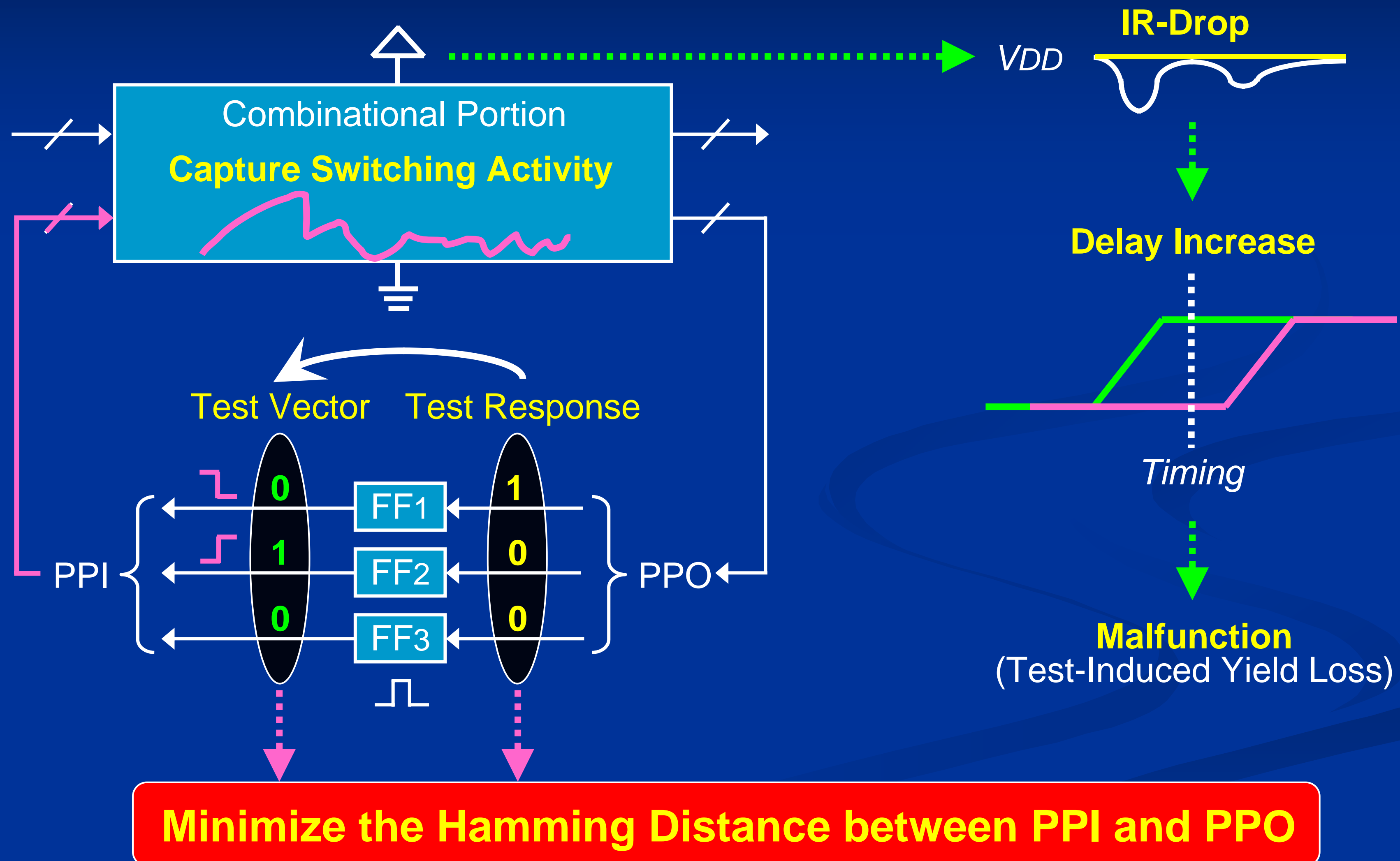
4. Capture Power Reduction



© X. WEN 2010. All Rights Reserved.

4. Capture Power Reduction

Basic Idea of Capture Power Reduction

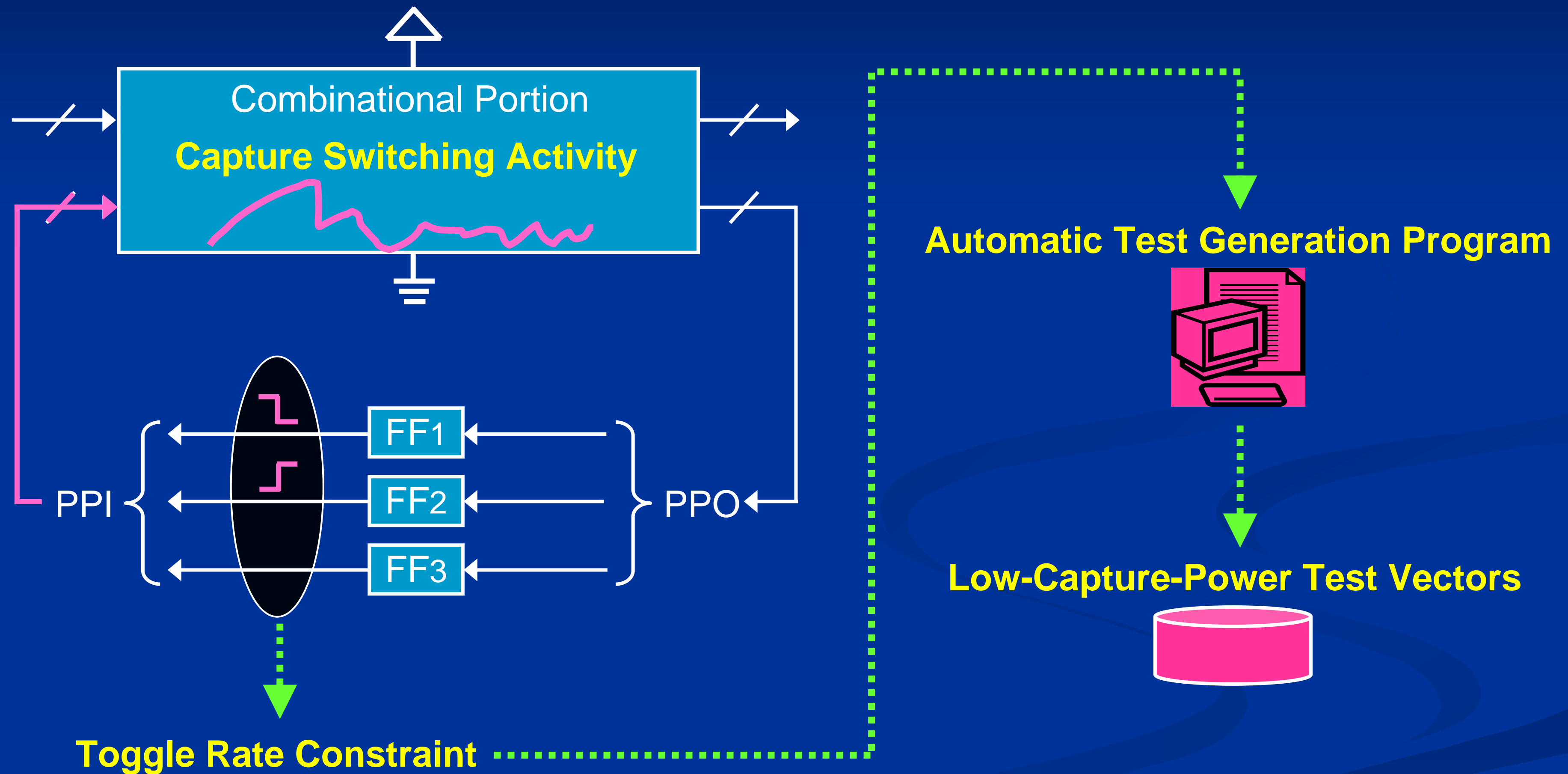


Minimize the Hamming Distance between PPI and PPO

© X. WEN 2010. All Rights Reserved.

4. Capture Power Reduction (SOFT)

The In-ATPG Approach

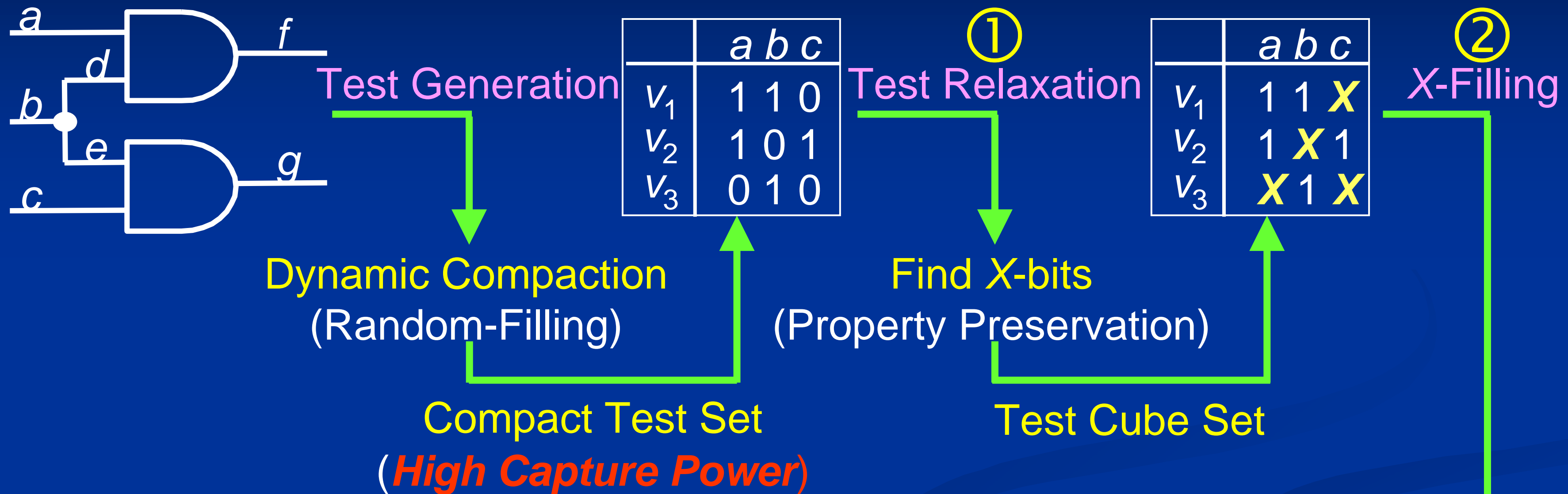


Easy to implement. / Severe test data increase.

© X. WEN 2010. All Rights Reserved.

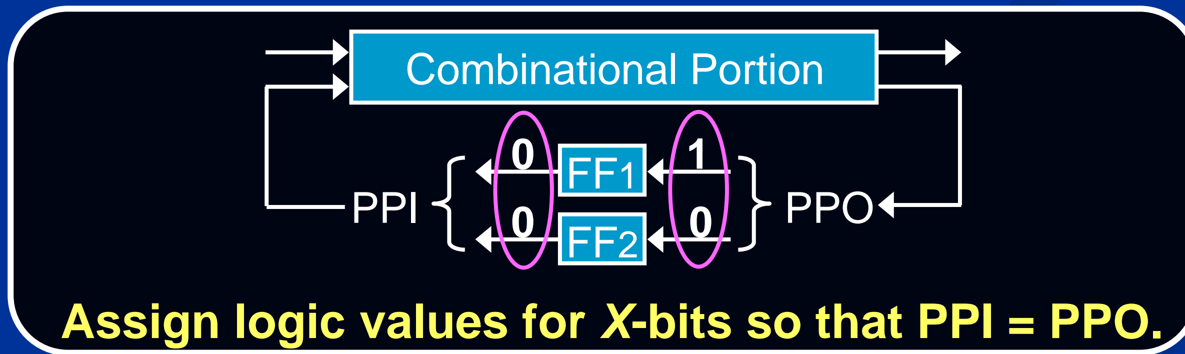
4. Capture Power Reduction (SOFT)

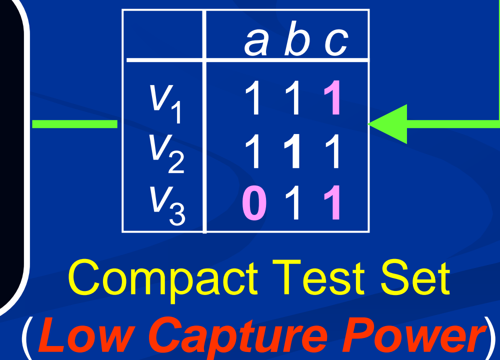
The Post-Test-Generation Approach



	a b c
v_1	1 1 0
v_2	1 0 1
v_3	0 1 0

	a b c
v_1	1 1 X
v_2	1 X 1
v_3	X 1 X





	a b c
v_1	1 1 1
v_2	1 1 1
v_3	0 1 1

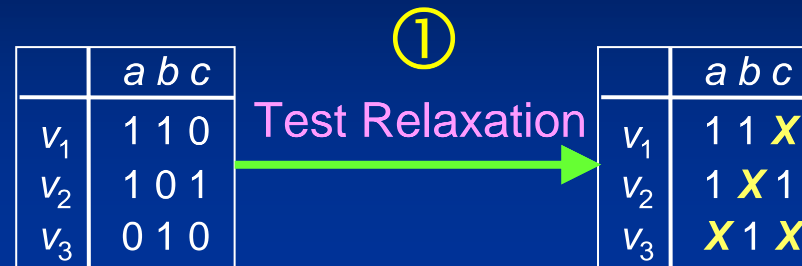
Compact Test Set
(*Low Capture Power*)

Easy to implement. / No test data increase.

© X. WEN 2010. All Rights Reserved.

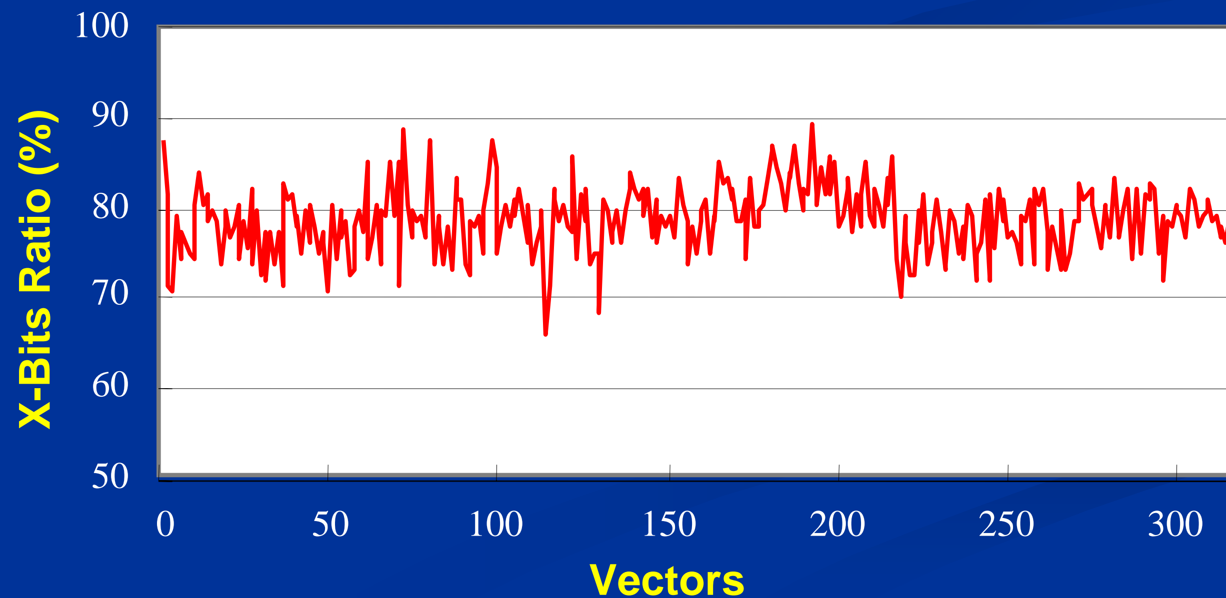
4. Capture Power Reduction (SOFT)

Example of Test Relaxation



Industrial Circuit

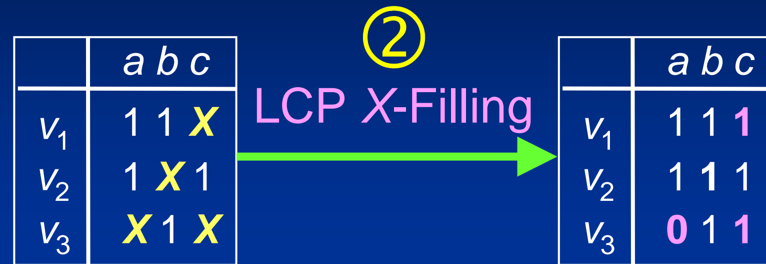
(90nm process / 1.2V / 50K gates / 2.5% VDD IR-drop budget)



© X. WEN 2010. All Rights Reserved.

4. Capture Power Reduction (SOFT)

Example of Low-Power-X-Filling



	a	b	c
v_1	1	1	X
v_2	1	X	1
v_3	X	1	X

	a	b	c
v_1	1	1	1
v_2	1	1	1
v_3	0	1	1

0-Prob
1-Prob
Test Cube v
f
f(v)
PI
PO
PPI PPO
(0.00, 1.00) → *a* 1
(1.00, 0.00) → *b* 0
(0.50, 0.50) → q_1 X / 0
(0.50, 0.50) → r_1 X / 1
0 *x*
1 *y*
X / 0 *z* ← *Justification*
X / 0 q_2 → (0.93, 0.07) → 0
X / 0 r_2 → (0.39, 0.61) → 1
Signal Probability Calculation
X Value Determination

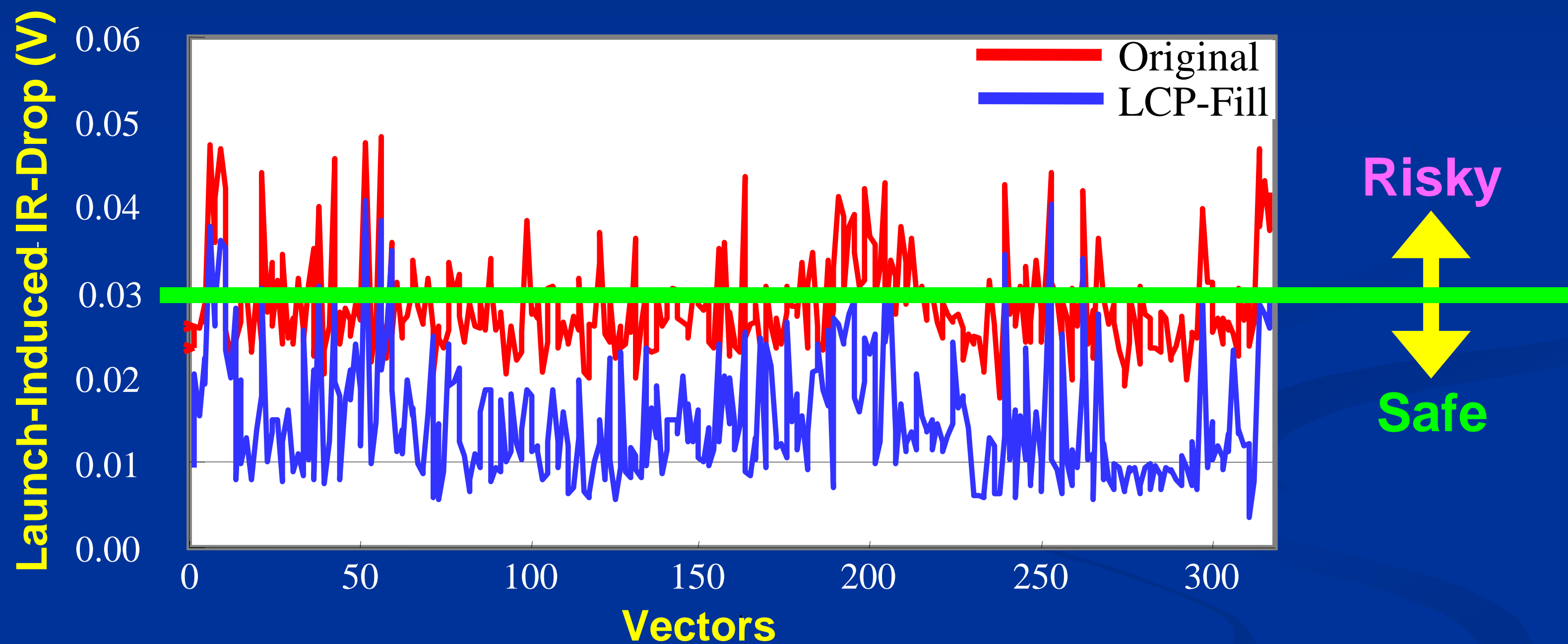
© X. WEN 2010. All Rights Reserved.

4. Capture Power Reduction (SOFT)

Effect of Low-Capture-Power X-Filling

Industrial Circuit

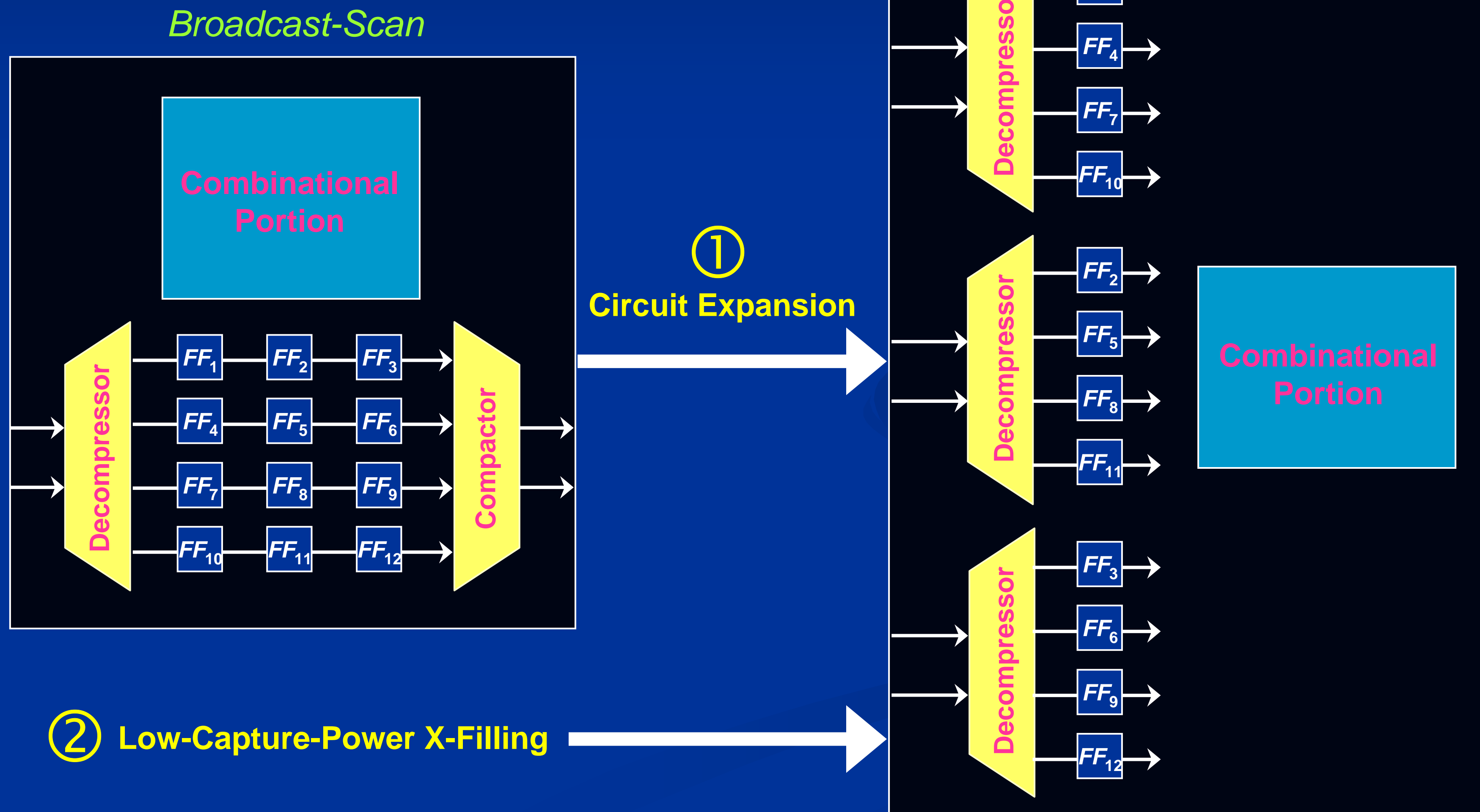
(90nm process / 1.2V / 50K gates / 2.5% VDD IR-drop budget)



© X. WEN 2010. All Rights Reserved.

4. Capture Power Reduction

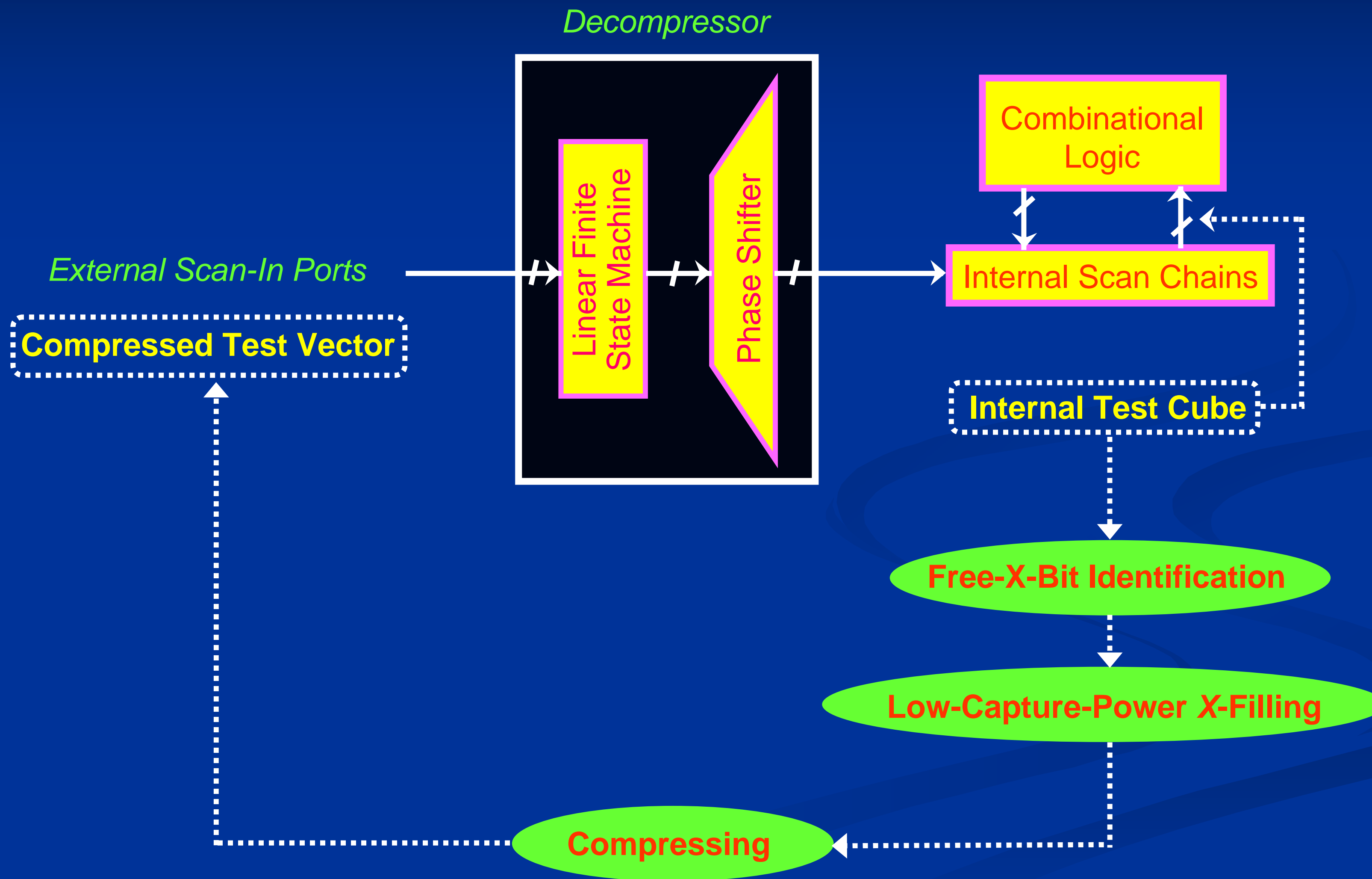
Extension to Compressed Scan Testing (Combinational)



© X. WEN 2010. All Rights Reserved.

4. Capture Power Reduction

Extension to Compressed Scan Testing (Sequential)



© X. WEN 2010. All Rights Reserved.

Outline

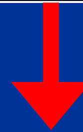
1. Risk of Low-Power LSI Circuits in Testing
2. Basic Strategy to Test Power Reduction
3. Shift Power Reduction
4. Capture Power Reduction
5. **New Research Opportunities**
6. Summary

© X. WEN 2010. All Rights Reserved.

5. New Research Opportunities

Where Are We Now ?

1. **The test power problem has become real and severe in industry.**
2. **Test power has been separated into shift power and capture power.**
3. **Simple metrics developed for test power analysis, ex. WSA.**
4. **Solutions developed for reducing average shift power.**
5. **Solutions developed for reducing peak capture power.**



Mission Accomplished ?

© X. WEN 2010. All Rights Reserved.

The Answer

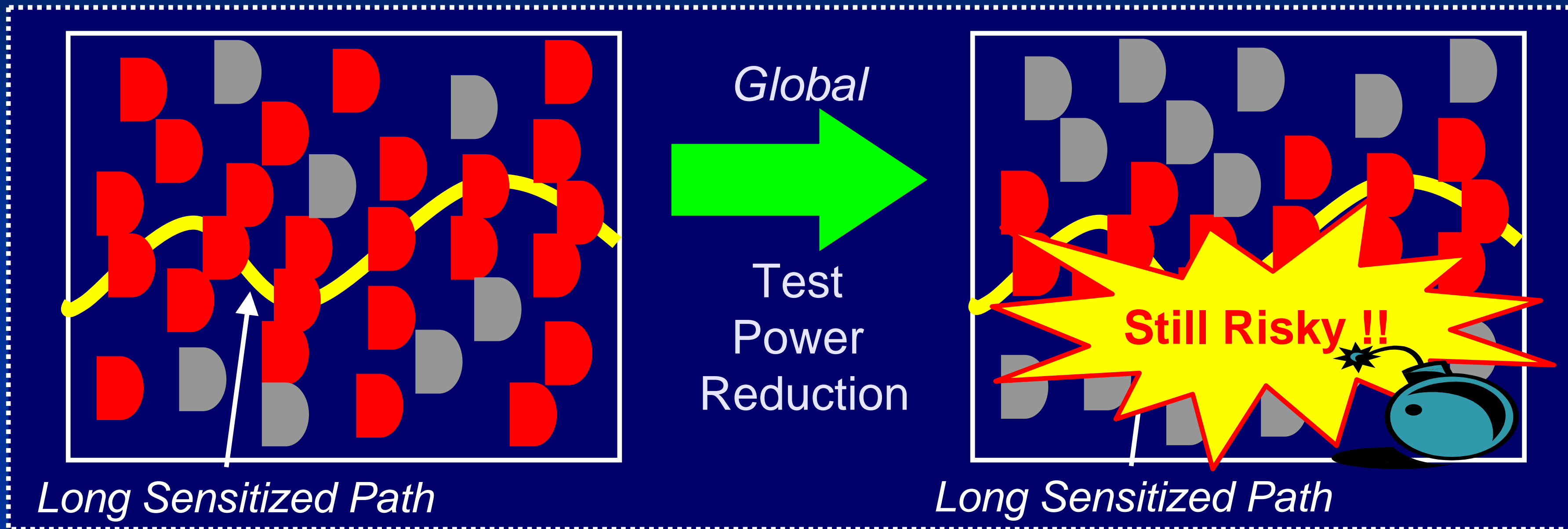
O

N

© X. WEN 2010. All Rights Reserved.

5. New Research Opportunities

Low-Power ≠ Power-Safety



Circuit	*# of Gates*	*# of FFs*	*# of Clock Gators*	*# of Test Vectors*	Test Power Analysis				
					# of Risky Test Vec.	*Ave. Sens. Paths / Vec.*	*Ave. Risky. Paths / Vec.*	*CPU (sec.)*	*# of Risky Vec. with Low WSA*
Small	50K	1,077	66	319	8	0.1	1.1	48	3
Large	600K	35,566	984	191	11	0.2	3.8	2,772	5

© X. WEN 2010. All Rights Reserved.

5. New Research Opportunities

Gold Rush Goes On

① Fast and accurate vector-based test power safety checking

② Mitigating the clock-skew impact of shift power

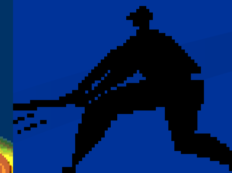
③ Pinpoint capture power management

④ Solution-independent migration framework for test compression

⑤ IP development with predefined low-power test data / infrastructure

⑥ High-quality low-shift-power & low-capture-power logic BIST

⑦ Power-safe 3D testing



More Gold Ahead

© X. WEN 2010. All Rights Reserved.

5. New Research Opportunity --- 1

Fast and Accurate Test Power Impact Analysis

Excessive Heat + Excessive Delay along Sensitized Paths

Heat Analysis

IR-Drop Analysis + Delay Analysis

Ideal but costly in terms of CPU time and data volume.

Sensitization Analysis

Severe impact of process variation.

S.O.S.

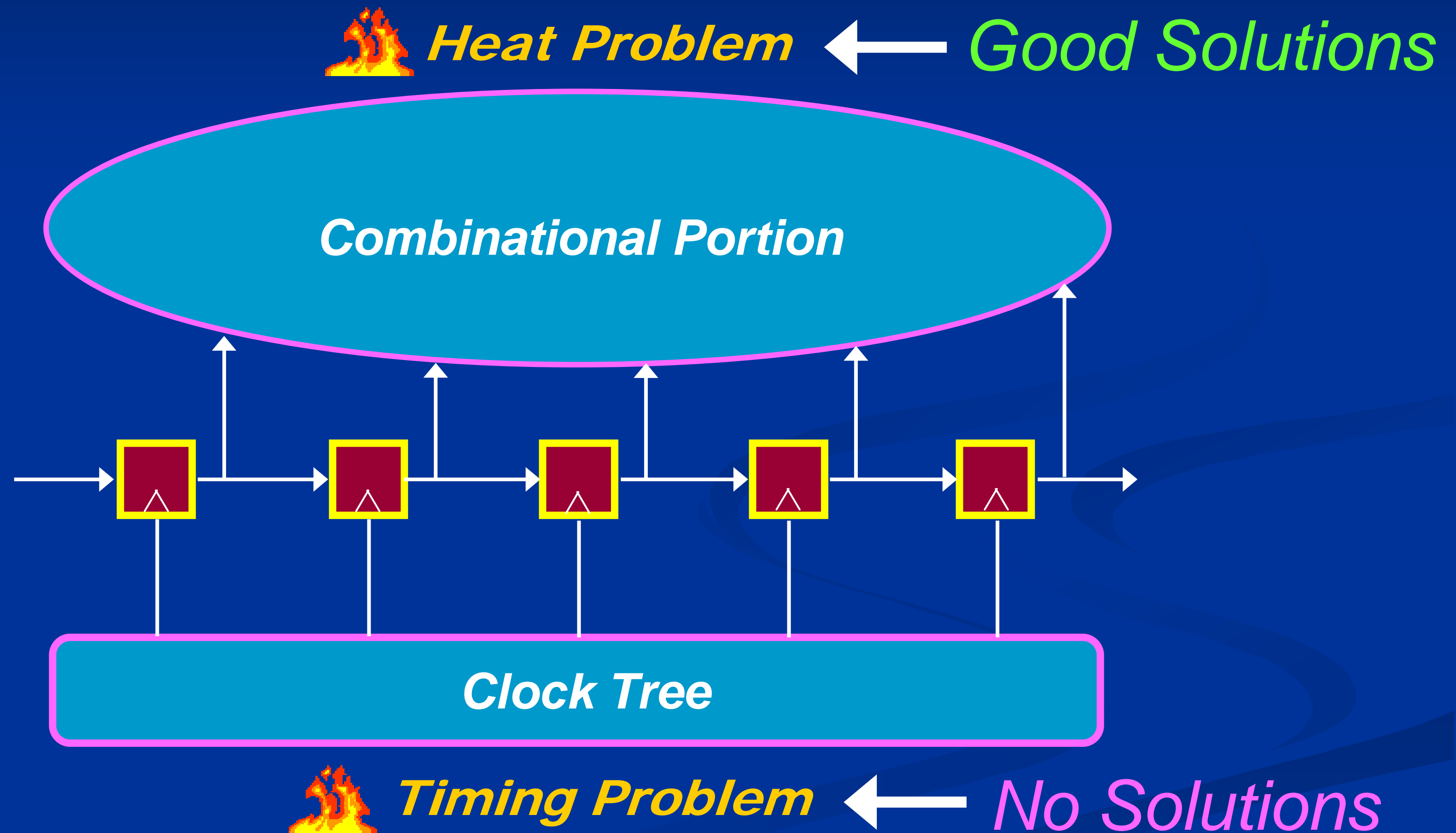
No one can predict whether a test vector is power-safe or not.

No one knows whether test power is sufficiently reduced or not.

© X. WEN 2010. All Rights Reserved.

5. New Research Opportunity --- 2

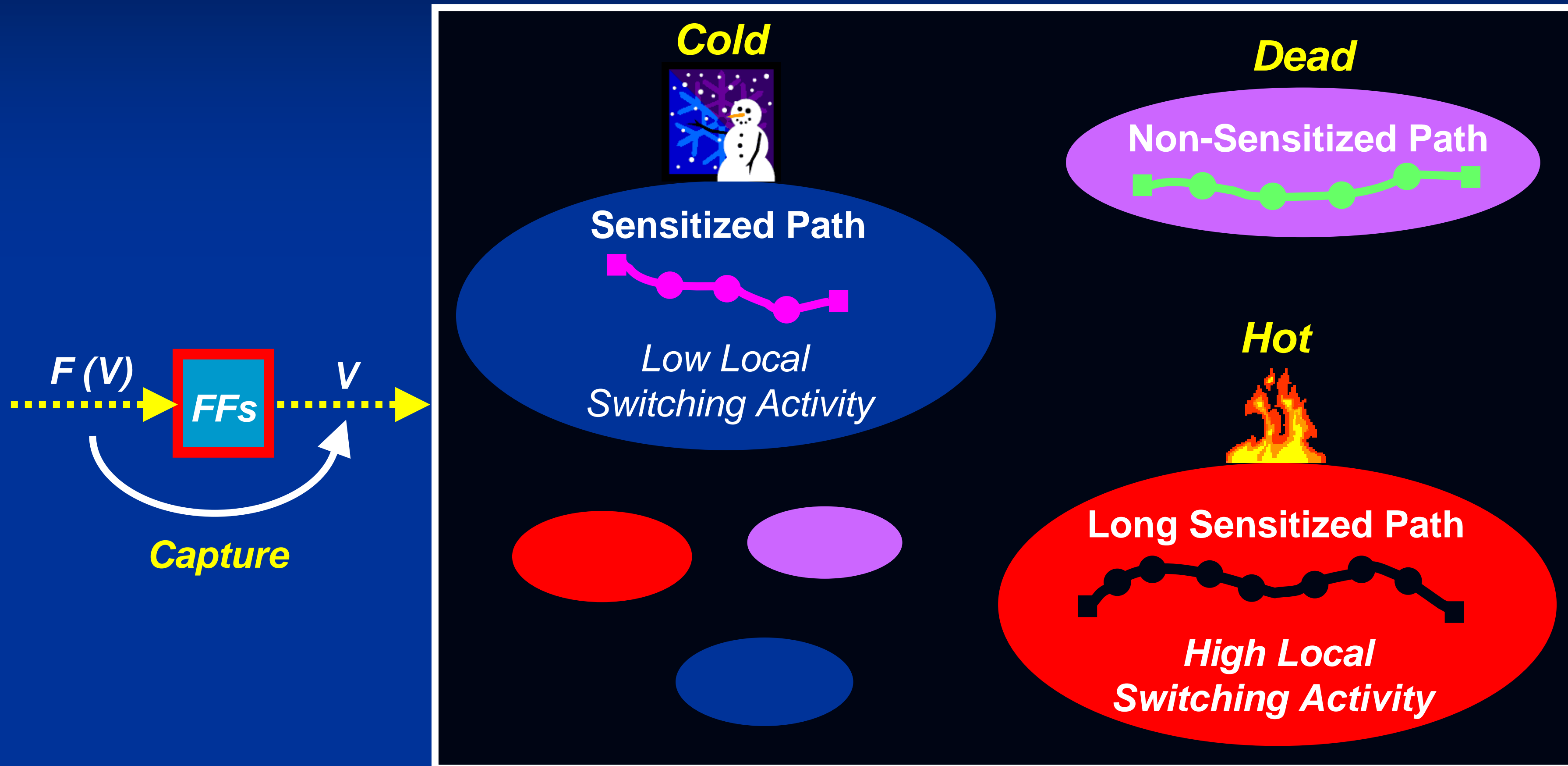
Mitigating the Clock-Skew Impact of Shift Power



© X. WEN 2010. All Rights Reserved.

5. New Research Opportunity --- 3

Pinpoint Capture Power Management



Right Power Test ← Pinpoint

- No need to consider ***dead areas***.
- ***Hot areas*** must be removed.
- ***Cold areas*** may be made "*warm*".

© X. WEN 2010. All Rights Reserved.

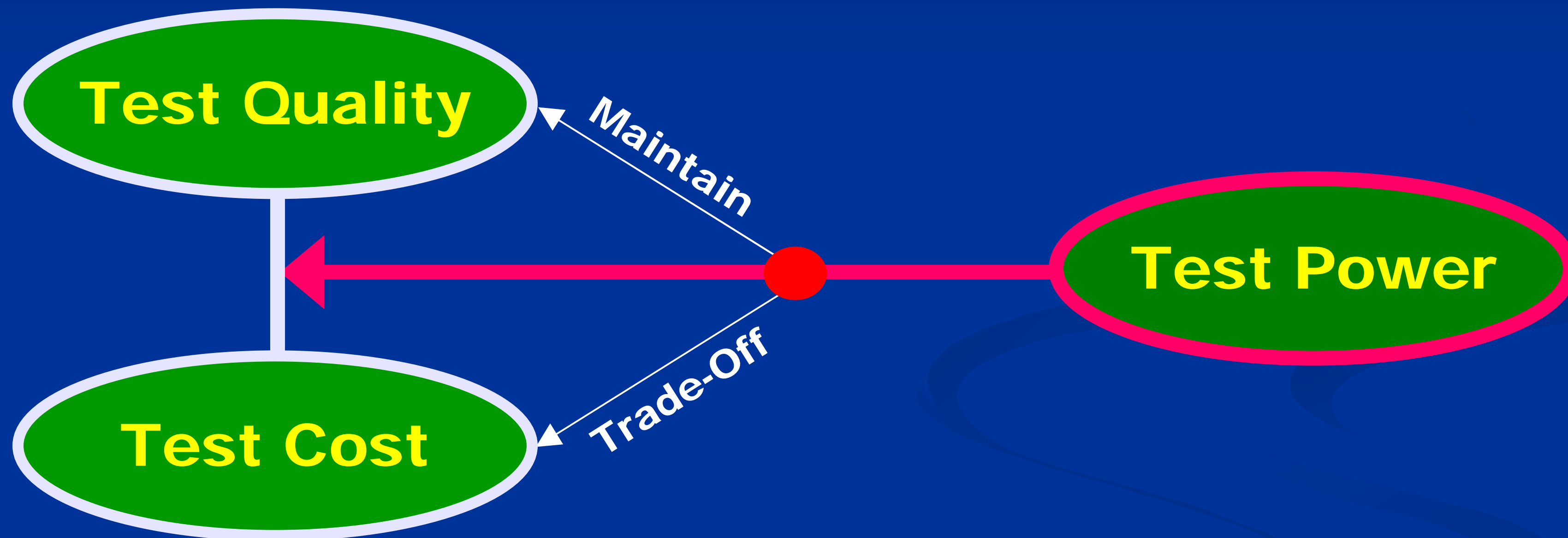
Outline

1. Risk of Low-Power LSI Circuits in Testing
2. Basic Strategy to Test Power Reduction
3. Shift Power Reduction
4. Capture Power Reduction
5. New Research Opportunities
6. **Summary**

© X. WEN 2010. All Rights Reserved.

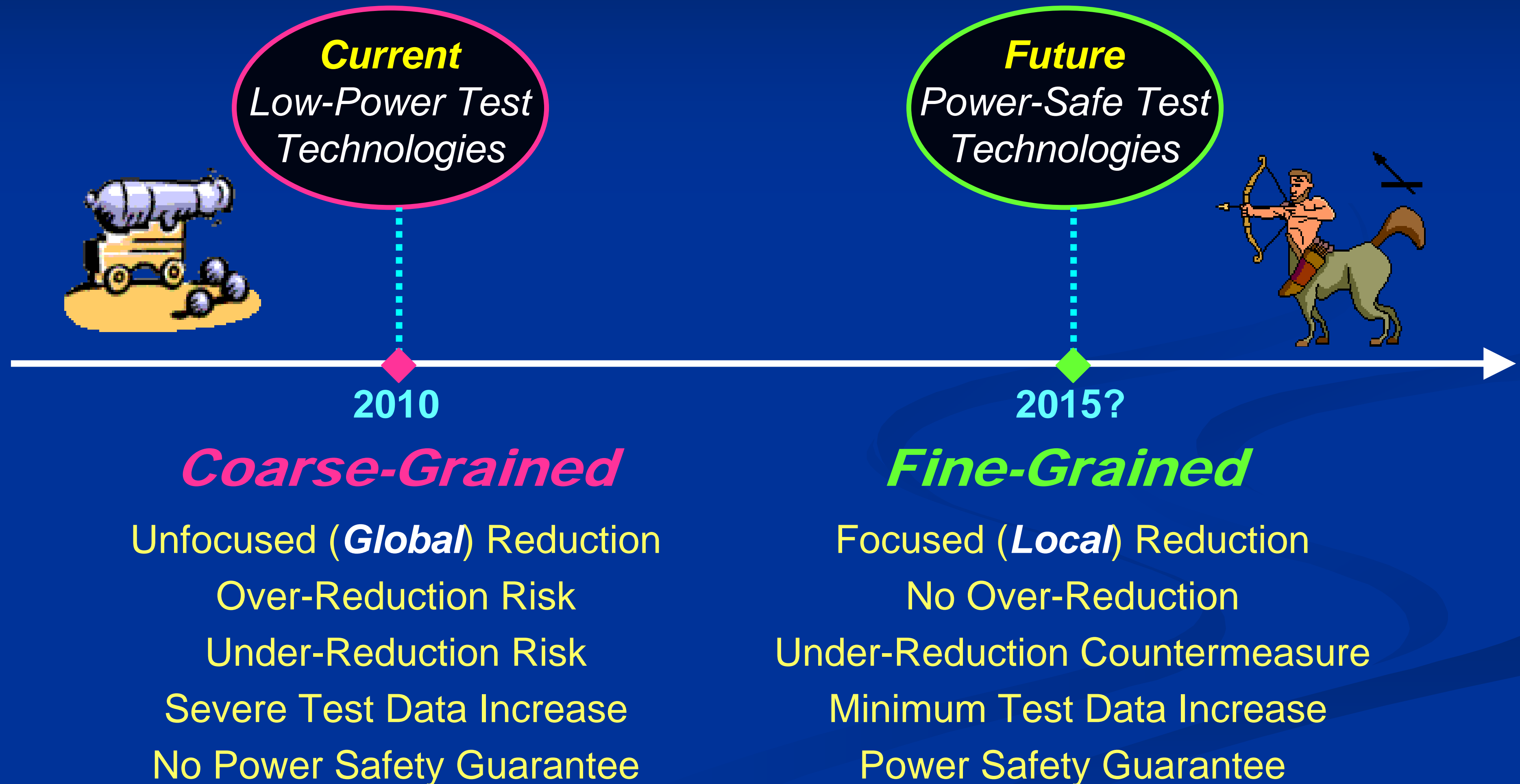
6. Summary

Holistic View



© X. WEN 2010. All Rights Reserved.

6. Summary



© X. WEN 2010. All Rights Reserved.

6. Summary

Basic Message

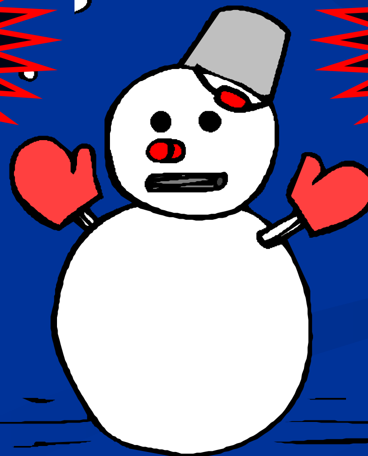
Functional Power (1x) ≠ Test Power (2x~5x)

Excessive Test Power → Test-Induced Yield Loss

↓

Low-power LSI circuits are at risk in testing !

Low - Power Design

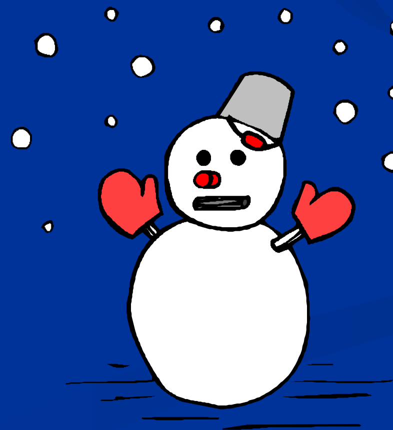


Low - Power Test

© X. WEN 2010. All Rights Reserved.

THANK YOU

*Let us make LSI testing "**cool** ".*



© X. WEN 2010. All Rights Reserved.